

A 2.7 μ W 10b 640kS/s Time-Based A/D Converter for Implantable Neural Recording Interface

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Abstract—In this paper, we propose a time-based, programmable-gain A/D converter allowing for an easily-scalable, and power-efficient, implantable, biomedical recording system. The converter circuit is realized in a 90 nm CMOS technology, operates at 640 kS/s, occupy an area of 0.022 mm², and consumes less than 2.7 μ W corresponding to a figure of merit of 6.2 fJ/conversion-step.

Keywords—A/D converter, neural recording interface, time-based signal processing.

I. INTRODUCTION

A multi-channel [1]-[3], implantable, neural recording systems enables the interaction with neural cells to facilitate early diagnosis, and predict intended behavior before undertaking any preventive or corrective actions. However, the space to host these systems is restricted to ensure minimal tissue damage, and tissue displacement during implantation. Furthermore, power density of the entire system (including the analog front-end, signal sorting, wireless telemetry, energy harvesting, etc.) is limited to 800 μ W/mm² [4] to prevent possible heat damage to the tissue surrounding the device (and subsequently, limited power consumption prolong the battery's longevity and evade recurrent battery replacements surgeries). More specifically, analog front-end has severe power consumption requirement (i.e., 5-10 μ W/channel) as it is mounted to the electrodes, and has short heat path to the neural tissues under recording. In addition, for high-performance neural prosthetic devices, the high-density, raw data rate recording is required. A 128-channel, 10-bit-precise digitization of neural waveforms sampled at 40 kHz generates ~ 51 Mbs⁻¹ of data; the power costs in signal conditioning, quantization and wireless communication all scale with the data rate.

In this paper, we propose a time-based A/D converter (ADC), allowing for a power- and area-efficient digitization of neural waveforms. The time-mode converters based on asynchronous ADCs [5], slope and integrating ADC [6], or pulse-position modulation [7] offer high resource efficiency in terms of power and area. In time-based methodology, conventional voltage and current variables are replaced by corresponding time differences between two rising edges as the time variables, and logic circuits substitute the large-sized and power-hungry analog blocks. In deep-submicron CMOS devices, even with the supply voltage reduction, time resolution is increased due to the decrease of gate delay [8].

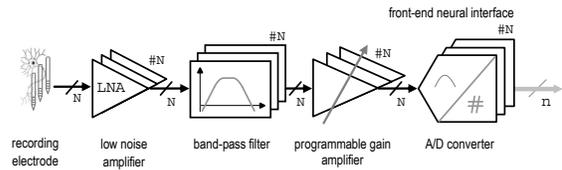


Figure 1: A N -channel front-end neural recording interface.

In the proposed design, a voltage signal is converted to a time-domain representation using a comparator-based switched-capacitor circuit [9] and a continuous-time comparator. To improve the power efficiency, resulting time domain information is converted to the corresponding digital code with a two-step time-to-digital converter (TDC), where fine quantization of the resulting residue is obtained with folding Vernier converter. The implementation results in a 90 nm CMOS technology show that a significant gain on throughput, resource usage and power reduction (less than 2.7 μ W corresponding to a figure of merit of 6.2 fJ/conversion-step) can be obtained for large-scale neural spike data, with a simple and compact ADC structure that has minimal analog complexity.

II. CIRCUIT DESIGN

A. Architectural Overview of a Multichannel Neural Interface

The data acquired by the recording electrodes in N -channel neural recording interface is conditioned using analog circuits, as illustrated in Figure 1. The electrode is characterized by its charge density and impedance characteristics (e.g., a 36 μ m diameter probe (1000 μ m²) may have a capacitance of 200 pF, equivalent to 40 k Ω impedance at 20 kHz), which determine the amount of noise added to the signal (i.e., 3.5 μ V_{rms} at 37°C). As a result of the small amplitude of neural signals (typically ranging from 10 μ V to 500 μ V and containing data up to ~ 20 kHz), and the high impedance of the electrode tissue interface, low-noise amplification (LNA), band-pass filtering, and programmable gain amplification (PGA) of the neural signals is performed before the signals can be digitized by the ADC. To relax the in-channel integration density, part of the front-end electronics, usually an ADC, is moved out of the channel to the periphery of the recording area (e.g., for the sampling rate of 40 kS/s for one channel to avoid extensive interpolation of spike samples, 640 kS/s ADC can be shared among 16 channels). Consequently, a 128-channel front-end interface can be built in 16 \times 8 configuration.

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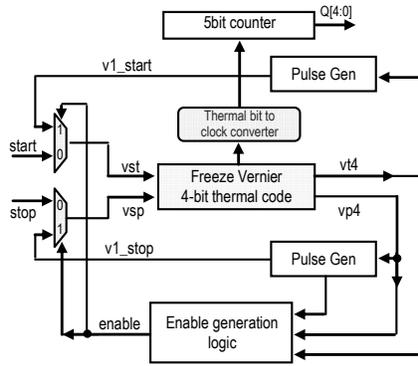


Figure 4: Block level of a folding Vernier delay time-to-digital converter.

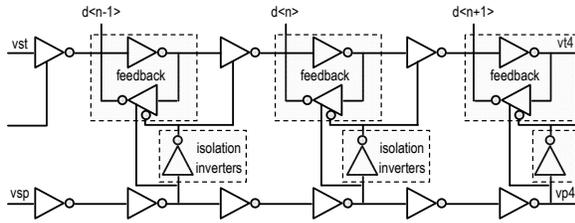


Figure 5: Simplified overview of a freeze Vernier delay line architecture.

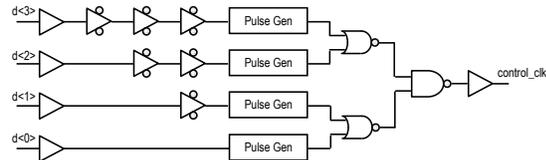


Figure 6: Thermal bit to clock generator.

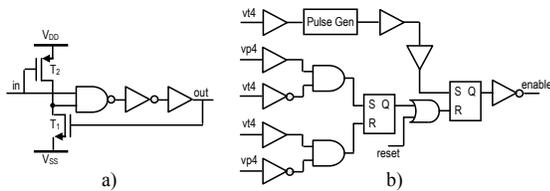


Figure 7: a) Pulse generator, b) the enable signal generation logic.

The synchronizer block, which consists of three flip-flops in series, ensures that the coarse and fine time measurements are correctly aligned.

A folding Vernier delay TDC is easily scalable to different time resolution and higher number of bits without increasing the area. The architecture achieves minimum time resolution of Vernier delay element (i.e. basic inverter delay), and, due to the folding, offers area-efficient solution. Instead of 32-element delay line required for the regular Vernier architecture, the folding feature allows the same Vernier delay stages to be used repeatedly to measure the delay. Additionally, with implemented dynamic control, we sequentially reduce the power required for each conversion.

Block level of a folding TDC is illustrated in Figure 4. Simplified overview of a freeze Vernier delay line architecture is shown in Figure 5. In our design, only four thermal codes

are generated at every cycle, and, hence, in the worst case, the measurement cycle is repeated eight times, which is equivalent to 32-bit thermal code with only four Vernier delay elements. The 4-bit thermal codes are converted into 4 pulses with thermal-to-clock generator (Figure 6), and clock a 5-bit counter at the output of TDC. For each thermal bit generated in a freeze Vernier delay line, a corresponding pulse is generated using pulse generator (Figure 7a). The distance between two pulses is controlled with current-starved inverters. Schematic of enable generation logic is illustrated in Figure 7b). For rising edge input, the circuit generates a pulse. The width of the pulse is determined by the nand gate, inverter and the buffer. The *enable* signal, which decides if either signals *start/stop* or *v1_start/v1_stop* continue into the next cycle, is generated using signals *vt4* and *vp4*. In the first conversion cycle, *enable*=0 and *vstart/vstop* is selected for measurement, otherwise *v1_start/v1_stop* is selected. The *enable* signal is switched from 1 to 0 when the rising edge of *vstart/v1_start* crosses the rising edge of *vstop/v1_stop*. This particular feature dynamically decides when the conversion is stopped, hence, power/conversion is optimized based on the input. The TDC also offers a feedback to the system with a *ready* signal (inverted signal of *enable*), indicating that it is ready for next conversion.

The 4-bit thermal code is generated with freeze Vernier architecture [12]. In the conventional Vernier architecture, time capture elements or early-late detectors (e.g. a D-register or an arbiter) impose the large load on the circuit. In the freeze Vernier TDC, the time capturing is instead performed by freezing the node voltages of the start line in a linear Vernier delay line, allowing a power- and area-efficient conversion. The freeze Vernier converter consists of inverters and current enabled inverters only. Additionally, the circuit does not require any reset signal - it resets on the falling edge of the stop and the start signal. The delays of the inverters in the freeze Vernier delay elements are controlled using bias current, thus, controlling the resolution of the TDC.

III. SIMULATION RESULTS

Design simulations on the transistor level were performed at body temperature (37 °C) on Cadence Virtuoso using industrial hardware-calibrated TSMC 90nm CMOS technology. The analog circuits operate with a 1 V supply, while the digital blocks operate at near-threshold from a 0.4 V supply. Spectral signature of ADC is illustrated in Figure 6a). The circuit offers a programmable amplification of 0-18 dB by digitally scaling the voltage-to-time converter. SNDR, SFDR and THD vs. sampling and input frequency is illustrated in Figure 6b) and 6c), respectively. The THD in the range of 40-640 kS/s is above 63 dB within the bandwidth of neural activity of up to 20 kHz; SNDR is above 58 dB, and SFDR more than 64 dB. The maximum simulated DNL is 0.6 LSB and the maximum simulated INL is 0.8 LSB. Variation across slow-slow and fast-fast corner is ± 0.35 ENOB.

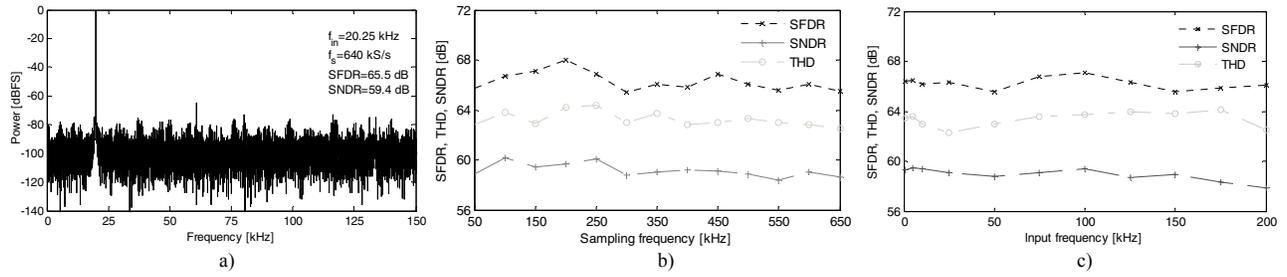


Figure 6: a) Spectral signature of A/D converter, b) SFDR, SNDR and THD vs. sampling frequency with $f_{in}=20$ kHz and gain set to 18 dB, c) SFDR, SNDR and THD vs. input frequency with $f_s=640$ kHz and gain set to 18 dB.

	[1]	[2]	[3]	[5]	[7]	[13]*	[14]*	[15]	[16]*	[17]*	[this work]*
Technology	0.18	0.18	0.18	0.12	0.09	0.18	0.09	0.18	0.35	0.09	0.09
Type	SAR	SAR	SAR	Time	Time	Current	SAR	$\Sigma\Delta$	SAR	SAR	Time
V_{DD} [V]	0.45	1	1.8	1.2	1	1.2	1	1.8	3.3	0.5	1
f_s [kS/s]	200	245	120	1000	1000	16	1000	50	16	1280	640 40
ENOB	8.3	8.3	9.2	10	7.9	8	9.34	10.2	8.9	9.95	9.4 9.5
FoM [fJ/conv-st]	21	109	382	175	188	132	2.87	0.22	93	2.36	6.2 21
Power [μ W]	1.35	8.4	27	180	14	0.45	1.79	13	3.06	3	2.7 1.6
Area [mm ²]	NR	NR	NR	0.105	0.06	0.078 [†]	NR	0.038	NR	0.048 [†]	0.022 [†]

TABLE I- COMPARISON WITH PRIOR ART - *SIMULATION DATA, NR - NOT REPORTED, [†]- ESTIMATED.

The VTC is >9 bit linear across 0.5 V input range. Consequently, ramp rate variation across the input range is limited to 10%, leading to 400 μ V nonlinear voltage variation across the output range. The reference clock frequency is 80 MHz, and, subsequently, the counter realizes a 5 bit resolution over the 400 ns TDC input time signal range. The ramp repetition frequency, i.e. sampling frequency of the proposed ADC, is 640 kHz. The simulated ENOB is 9.4 bits over the entire neural spikes input bandwidth. The total A/D converter consumes 2.7 μ W, when sampled at 640 kS/s, and 1.6 μ W at 40 kS/s, respectively. The area of the folding Vernier TDC design sums up to 10.5 μ m², the average resolution is 10.05 ps, it operates at a power supply of 0.4 V, and consumes 0.6 μ W of power at 640 kS/s sampling rate. Table I summarize the performance and comparison with previous art, with figure of merit calculated according to $FoM=P/(2f_{in}\times 2^{ENOB})$ [J/conv-st].

IV. CONCLUSION

In this paper, a low-power, time-based, programmable-gain A/D converter for multi-channel integrated neural implant front-end consuming less than 2.7 μ W is presented. The power consumption is scaled with the input voltage level making the circuit suitable for low energy signals. The circuit realized in 90 nm CMOS technology, which embeds both PGA and ADC functionalities, with 6.2 fJ/per conversion exhibits one of the best FoM reported, and occupy an estimated area of only 0.022 mm².

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