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ADC Multi-Site Test Based on a Pre-test with Digital Input Stimulus

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Abstract This paper describes two novel algorithms based on the time-modulo reconstruction method intended for detection of the parametric faults in analogue-to-digital converters (ADC). In both algorithms, a pulse signal, in its slightly adapted form to allow sufficient time for converter settling, is taken as the test stimulus relieving the burden placed on the accuracy requirement of the excitation source. Instead of calculating the accurate conventional dynamic and static parameters, a signature result is obtained through the analysis of the output data in the time domain. The basic concept of the algorithms is the evaluation on the performance of ADCs by the comparison of the similarity of the output waveforms. The multi-site test is expensive for traditional specification-based tests of ADCs, as high quality analogue data generators are required. Based on these two algorithms, this paper proposes a solution for this problem. The objective of the test scheme is not to completely replace traditional specification-based tests, but to provide a reliable method for early identification of excessive parameter variations in production test that allows quickly discarding of most of the faulty circuits before performing a conventional test. The efficiency of the methods is validated on an industrial 12-bit pipelined ADC both in simulations and in measurements.

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1 Introduction

The conventional specification test of an ADC contains dynamic and static tests. Typically a dynamic test is for testing total harmonic distortion (THD), signal-to-noise-ratio (SNR), spurious-free-dynamic-range (SFDR), second harmonic and third harmonic power. A static test is to test integral non-linearity (INL), differential non-linearity (DNL), gain and offset. For the specification-based test, a sine wave or a ramp signal is used to test the dynamic or static parameters. The requirement of the quality of test signals depends on the specifications of the ADC under test [1].

Nowadays, multi-site test is a widely used approach in production test. It can reduce the average testing time per device-under-test (DUT) by testing multiple devices on the same test head simultaneously [12]. Nevertheless, for an ADC test, the increasing number of DUTs in parallel usually requires expensive high-quality analogue signal sources. This requirement causes difficulty in implementing multi-site test with regard to the ADC test.

To solve this problem, several research approaches have been investigated to further decrease the cost or the requirement of the accurate analogue stimulus generators for ADC testing. A new method for estimating the INL errors of ADCs is proposed in [2]. Instead of using the Histogram method, it calculates the transition levels of the ADC transfer function. The method can accurately estimate the INL of ADCs without requiring any particular input test signal. In [8], the author presents a new high-precision ramp signal generator for low-cost ADC static testing.

With the proposed test method, the ADC can be tested on general digital testers. A traditional ramp generator is combined with an operational amplifier. The new set-up of the ramp generator can test an ADC up to 14 bits. In [9], a staircase-like exponential waveform is used as the test input signal; it is generated by a pulse-width modulation (PWM) signal followed by an off-chip *RC* filter. With this method, the *3*rd harmonic distortion of an ADC up to 20-bits can be tested with a 3rd order polynomial fitting algorithm. The accuracy of the result is primarily limited by the linearity of the off-chip capacitor. The authors in [3] explored the approximation of a multi-tone signal to test the high-speed ADC using the alternate test approach. Testing the dynamic parameters of the high-speed ADC requires a faster and more accurate signal generator, which increases the production testing cost. The multi-tone signal is generated by using a low-frequency source available on a low-cost tester. By applying a regression-based function obtained from the training data, the specification results can be obtained from the bench testing with a multi-tone test stimulus. The references [5–7] are continuous works investigating how to use a low-linearity ramp signal to test high resolution ADCs by a stimulus error identification and removal (SEIR) algorithm. In this algorithm, two non-linear ramp signals with certain offset are applied sequentially as the test stimulus. As a result, a 16-bit ADC can be tested to one least-significant-bit (LSB) accuracy by two 7-bit linear ramp signals.

Reference [4] proposes the Modulo Time Plot, which reconstructs the output waveform of the ADC from a number of periods into only one period. It is useful for quick visual inspection of the performance of the ADC. It is used in conventional ADC testing. The test method proposed in this paper also exploits this technique to analyze output data.

With the advance of CMOS technology, more and more ADCs are integrated into platform-based designs, which are mostly used for video, audio and high-speed communication systems. A pulse signal is obviously easy to generate on such platform-based designs, whose standardized architecture is usually composed of memories, RF and mixed-signal front ends and importantly, many multiple-processor cores. This work exploits an adapted pulse signal as the test stimulus. Two new post-processing algorithms are proposed. We give a course-grain solution for ADC multi-site testing based on the algorithms. As the test stimulus and post-processing algorithm of this method are very suitable for multi-site testing, the test is supposed to be a quick pre-test filtering out the faulty devices before specification testing. As a result, only the devices passing the pre-test are needed to be tested by the complicated specification test. Especially when the yield is moderate, it can reduce the production test costs significantly.

2 Detection by Using a Pulse Signal

An adapted pulse signal can be expressed in the time domain as:

$$\begin{aligned} x(t) &= \frac{A}{T_r} t(u(t) - u(t - T_r)) \\ &+ A(u(t - T_r) - u(t - (T_r + T_h))) \\ &+ A\left(1 + \frac{T_h + T_r - t}{T_f}\right)\left(u(t - (T_r + T_h)) - u\left(t - T_r + T_h + T_f\right)\right) \end{aligned} \tag{1}$$

, where A, T_r, T_f and T_h denote the amplitude, rising and falling times of the signal and time while being of high-level, respectively. The spectrum of an adapted pulse signal can be found as:

$$\begin{aligned} F\{x(t)\} &= \tfrac{A}{\omega^2 T_r}\left(e^{-j\omega T_r} - 1\right) - \tfrac{A}{\omega^2 T_f}\left(e^{-j\omega T_h} - 1\right)e^{-j\omega(T_r + T_h)} \\ &- \tfrac{2jA}{\omega^2 T_r} \sin\omega\tfrac{T_r}{2} e^{-j\omega\frac{T_r}{2}} + \tfrac{2jA}{\omega^2 T_f} \sin\omega\tfrac{T_f}{2} e^{-j\omega\left(T_r + T_h + \frac{T_f}{2}\right)} \end{aligned} \tag{2}$$

One can see that the spectral representation of an adapted pulse signal is not only a function of the sampling frequency and amplitude of the signal, as for sine- wave stimuli, but a periodic function of a pulse rising and falling times as well. As a consequence, its power spectrum contains more redundant frequency components than a sine wave. When combined with the non-linear response of the ADC under test, well-controlled and accurate determination of ADC's parametric faults through conventional methods become complex and time excessive [10].

In our case, the time- domain analysis is explored to detect the parametric faults in an ADC with a pulse-wave input signal. Instead of obtaining the accurate specification results, a signature result to decide whether the DUT passes or fails the test is calculated from the time-domain analysis. The basic concept of our method is that by comparing the results' similarity between the digital outputs of the golden device and the DUT, one can detect the faulty devices from a large amount of DUTs in a multi-site test environment. The transfer function of a 3-bit ideal ADC is shown in Fig. 1. One can see that the ideal ADC is perfectly linear and only contains the quantization error, which is determined by the resolution. If the same test stimuli are applied to two ideal ADCs with the same transfer function, their outputs are expected to be the same as well. In the real world, the ADCs with the same design will have similar but different transfer functions, as there are also other types of errors like gain, offset, differential linearity errors and so on, caused by the process of fabrication. In this case, the

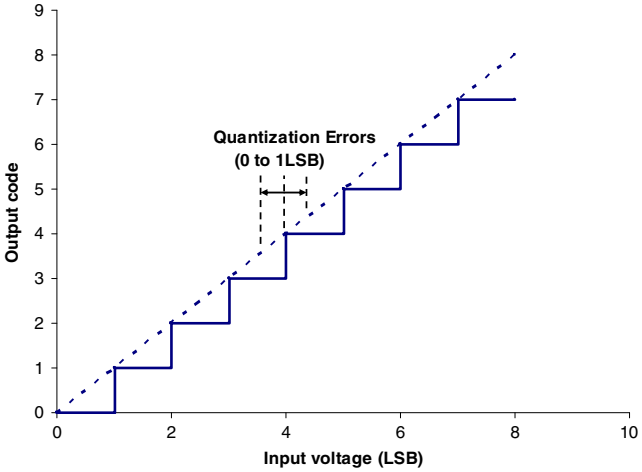

Fig. 1 Ideal transfer function of a 3-bit ADC

transfer functions will be more different from the ideal one as there are more errors in an ADC. As a result, the output will have more variation as well with the same input stimuli. In this way, the similarity of the outputs between the golden devices and the DUT can reflect the faults in the DUT. A certain amount of golden devices are used to generate the acceptable range of the output by considering the process variations of the fabrication process.

A simple and fast pre-test can be carried out by this method before testing the specific dynamic and static parameters of the ADC. The faulty devices can be discarded by this pre-test. Hence the number of devices, which are tested by the complicated and time-costly conventional test, will be reduced efficiently. As a result, it will reduce the test time when there is a large volume of DUTs to be tested. The test flow of this proposed method including both pre-test and ADC specification test is shown as follows:

- Step1: Apply pre-test to all the DUTs in the multi-site test environment
- Step 2: Discard the faulty devices defined in step 1
- Step 3: Apply the specification test to the remaining devices

The rising and falling edges of the pulse signal are the crucial parts of the input signal for ADC testing. If a pulse signal with infinite small rise time (T_r) or fall time (T_f) is applied to an ADC, the output of the ADC will be only given the digital codes representing the low and high levels of the pulse. Hence it provides too limited information to evaluate the performance of the ADC. Based on the Nyquist theory [1], the T_r and T_f should be at least larger than the reciprocal of the sampling frequency of the ADC.

In both of the algorithms, a modulo time plot technique [4] is applied to reorder the ADC's output to enable the time-domain results easier to process. By using this technique, a number of periods of the output are converted into one single period which still includes the same test information as the original output in the time domain. After applying this algorithm, the output of the ADC is converted from a several-periods pulse signal into a one-period pulse signal. The reconstructed waveform shows the errors of the ADC in a more clear way [4]. As an example, the time sequential plot of a pulse signal sampled by a 6-bit ADC is shown in Fig. 2. The x-axis denotes the number of samples in time sequential while the y-axis denotes the output amplitude. The frequency of the input pulse signal is f_{in}=7 MHz, the sampling frequency is f_s=300 MHz and the number of samples is N_s=3002. After applying the modulo time plot technique, the reconstructed pulse signal is shown in Fig. 3. It clearly shows that the sampled signal is a pulse signal as in contrast with Fig. 2.

2.1 Deviation Comparison by Using the Amplitude of the ADC Output

The overview flow of the algorithm is shown in the following Tables 1 and 2.

Initialization and data collection As shown in Fig. 4, in order to obtain the fault-free range of the pre-test, a pulse wave test stimulus is applied to a collection of golden devices with all the corner cases (such as fast and slow cases). The golden devices are a collection of the examples of the fault-free devices defined by the specification test. Subsequently, the pulse wave stimulus with the same amplitude, duty cycle, frequency, rising and falling edges will be applied to all the DUTs.

Step 1 Apply the technique of modulo plot [4] to the output of the golden devices. After reconstruction

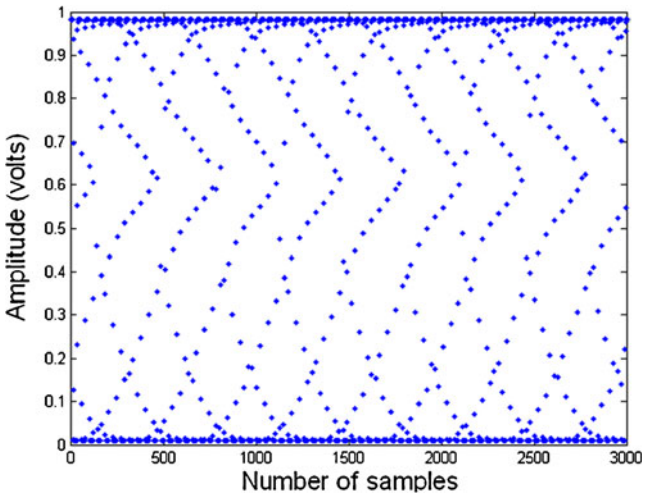

Fig. 2 The plot of pulse signal samples in time sequential

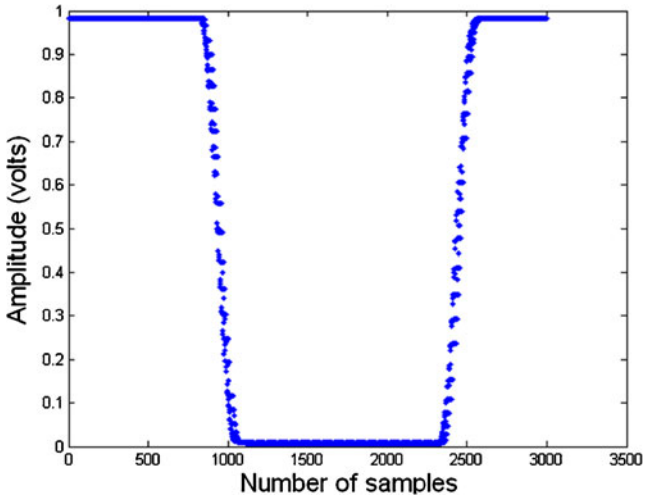

Fig. 3 Modulo time plot for Fig. 2

by the modulo plot, the reordered output is shown as Fig. 4. The x-axis denotes the number of samples while the y-axis denotes the amplitude of the output.

Step 2 Divide the one-single period reconstructed output into 4 sections as shown in Fig. 4. The start of the sampling and the end of the sampling point of each section are not required to be selected very accurately. However, all the golden devices must have the same starting and ending points. For each section, an array of amplitudes *Am* can be obtained. Each element *Am (i)* represents the amplitude of one sampling point. As discussed before, the rising and falling edges responses contain the most important test information from the ADCs.

Step 3 Determine the maximum value $Am_{\max}$ *(i)* and minimum value $Am_{\min}$ *(i)* of each element *Am (i)*. They are determined by comparing the values of *Am(i)* of all the golden devices' outputs.

Step 4 Apply step 1 and 2 to all the DUTs. When dividing the output into 4 sections, the starting and ending sampling points must be the same as the golden devices. Similar to *Am*, an array of the amplitude Am_{DUT} of the sampling points can be obtained from the reconstructed output.

Step 5 For each element Am_{DUT} *(i)*, it is verified whether it is within the acceptable range $[Am_{\min}$ *(i)*, $Am_{\max}$ *(i)]*. If Am_{DUT} *(i)* > $Am_{\max}$ *(i)*, the amplitude deviation ΔAm *(i)* is defined as:

$$\Delta Am(i) = Am_{DUT}(i) - Am_{\max}(i) \tag{3}$$

Similarly, if Am_{DUT} *(i)* < $Am_{\min}$ *(i)*, we define the amplitude deviation $\Delta Am(i)$ as:

$$\Delta Am(i) = Am_{\min}(i) - Am_{DUT}(i) \tag{4}$$

For the case that Am_{DUT} *(i)* is within the acceptable range $[Am_{\min}$ *(i)*, $Am_{\max}$ *(i)]*, the amplitude deviation ΔAm *(i)* is defined as *0*.

Step 6 After collecting the amplitude deviation of all the sampling points of each section, the average out-of-

Table 1 The overview flow of the algorithm comparing the deviation by amplitude

Algorithm 1
Initialization
- Initialize the amplitude array *Am* of each sampling point
- Initialize the input stimuli
Data collection
- Collect *N* sampling points instants for each calculation
Main Body
1. Calculate the reconstructed output of the golden devices
2. Divide reconstructed output into four sections
3. Obtain the acceptable range of the output amplitude $[Am_{\min}(i), Am_{\max}(i)]$
4. Apply step 1 and 2 to DUTs to obtain Am_{DUT}
5. If $Am_{DUT}(i) > Am_{\max}(i)$ obtain $\Delta Am(i) = Am_{DUT}(i) - Am_{\max}(i)$
If $Am_{DUT}(i) < Am_{\min}(i)$ obtain $\Delta Am(i) = Am_{\min}(i) - Am_{DUT}(i)$
If $Am_{\min}(i) < Am_{DUT}(i) < Am_{\max}(i)$ obtain $\Delta Am(i) = 0$
6. Increase the index, *i*, and repeat previous step for best estimate
7. Calculate the out-of-amplitude-range percentage *P_am*

Table 2 Overview of flow of the algorithm comparing the deviation by angle

Algorithm 2
Initialization
- Initialize the angle array $\angle\varphi$ of each sampling point
- Initialize the input stimuli
Data collection
- Collect *N* sampling points instants for each calculation
Main Body
1. Calculate the reconstructed signal of the golden devices
2. Divide reconstructed output into four sections
3. Obtain the acceptable range of the angle deviation $[\angle\varphi_{\min}(i), \angle\varphi_{\max}(i)]$
4. Apply step 1 and 2 to DUTs to obtain $\angle\varphi_{DUT}$
5. If $\angle\varphi_{DUT}(i) > \angle\varphi_{\max}(i)$ obtain $\Delta\angle\varphi(i) = \angle\varphi_{DUT}(i) - \angle\varphi_{\max}(i)$
If $\angle\varphi_{DUT}(i) < \angle\varphi_{\min}(i)$ obtain $\Delta\angle\varphi(i) = \angle\varphi_{\min}(i) - \angle\varphi_{DUT}(i)$
If $\angle\varphi_{\min}(i) < \angle\varphi_{DUT}(i) < \angle\varphi_{\max}(i)$ obtain $\Delta\angle\varphi(i) = 0$
6. Increase the index, *i*, and repeat previous step for best estimate
7. Calculate the out-of-angle-range percentage $P\angle\varphi$

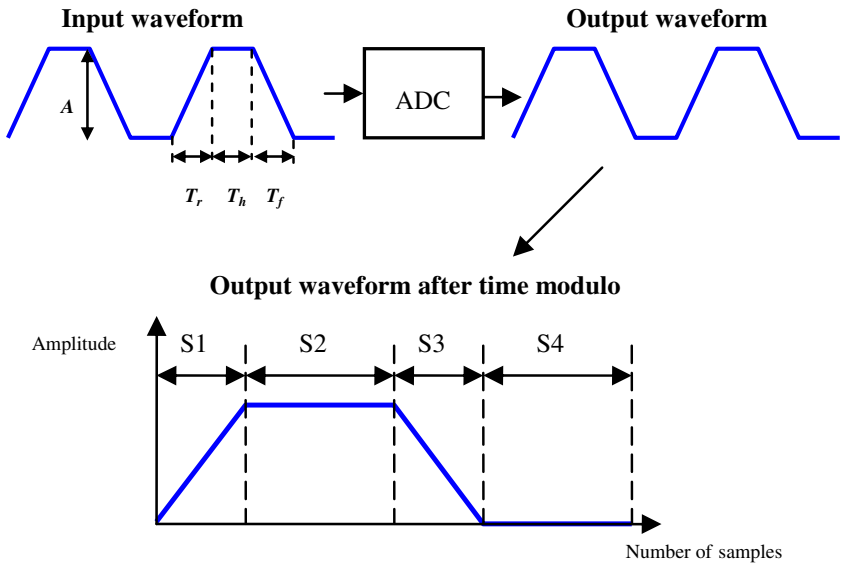

Fig. 4 The reconstructed pulse signal of the ADC output

amplitude-range percentage *P_am* of each section is calculated as:

$$P\_am = \frac{\sum_{i=1}^{N} \Delta Am(i)}{\sum_{i=1}^{N} Am_{\max}(i) - \sum_{i=1}^{N} Am_{\min}(i)} \quad (5)$$

N is denoted to be the total number of sampling points of each section. *P_am* is employed to evaluate the faults in the ADC, which will be shown later on.

2.2 Deviation Comparison by Using the Angle of the ADC Output

As shown in Fig. 5, the *i-1, i* and *i+1* points are three adjacent points on the output curve. If one connects two adjacent points *i* and *i-1* with a straight line, then an angle $\angle\varphi$ *(i-1)*, which is between the connected line and x-axis, can be obtained. In this way, with a curve of *N* sampling points, an array of angles $\angle\varphi$ *(1)*, $\angle\varphi$ *(2)*…$\angle\varphi$ *(i)*…$\angle\varphi$ *(N-1)* can be obtained, which describes the deviation of the *trend* of a curve. Compared with the previous algorithm, we use the angle deviation to evaluate the performance of the ADCs instead of amplitude deviation.

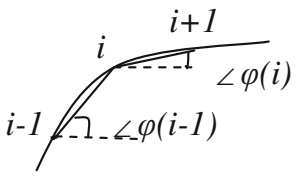

Fig. 5 The sampling points on the output curve of the ADC

An overview of the flow of the algorithm is shown in the following table:

The initialization and data collection are completely the same as the previous algorithm. So they will not be explained in detail again.

Step 1 Apply the technique of modulo plot [10] to the output of the golden devices.

Step 2 Divide the reconstructed output waveform into 4 sections in the same way as the step 2 of the previous algorithm. Similar to the *Am*, an array of angles $\angle\varphi$ can be obtained from each section of the output curve.

Step 3 By comparing $\angle\varphi$ *(i)* of all the corner cases, the maximum value $\angle\varphi_{\max}$ *(i)* and minimum value $\angle\varphi_{\min}$ *(i)* can be obtained for each element $\angle\varphi$ *(i)*.

Step 4 Apply step 1 and 2 to all the DUTs. An array of the angle $\angle\varphi_{DUT}$ of the sampling points from the DUT output can be obtained in the same way as in Step 2.

Step 5 For each element $\angle\varphi_{DUT}$ *(i)*, it is verified whether it is within the range *[*$\angle\varphi_{\min}$ *(i),* $\angle\varphi_{\max}$ *(i)]*.

If $\angle\varphi_{DUT}$ *(i)* > $\angle\varphi_{\max}$ *(i),* the angle deviation $\Delta\angle\varphi$ *(i)* is defined as:

$$\Delta\angle\varphi(i) = \angle\varphi_{DUT}(i) - \angle\varphi_{\max}(i) \quad (6)$$

For the case $\angle\varphi_{DUT}$ *(i)* < $\angle\varphi_{\min}$ *(i),* we define the angle deviation $\Delta\angle\varphi(i)$ as:

$$\Delta\angle\varphi(i) = \angle\varphi_{\min}(i) - \angle\varphi_{DUT}(i) \quad (7)$$

If φ_{DUT} *(i)* is within the range *[*$\angle\varphi_{\min}$ *(i),* $\angle\varphi_{\max}$ *(i)]*, the angle deviation $\Delta\angle\varphi$ *(i)=0.*

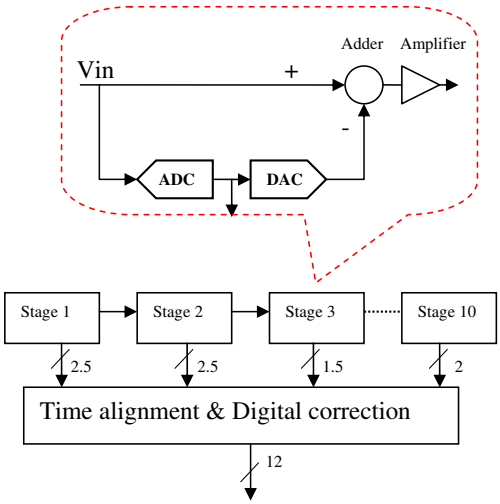

Fig. 6 The basic structure of a 12-bit pipelined ADC

Step 6 Finally, the average out-of-angle-range percentage $P\angle\varphi$ of the whole curve is found as:

$$P\angle\varphi = \frac{\sum_{i=1}^{N-1} \Delta\angle\varphi(i)}{\sum_{i=1}^{N-1} \angle\varphi_{\max}(i) - \sum_{i=1}^{N-1} \angle\varphi_{\min}(i)} \quad (8)$$

, where N is the total number of sampling points in each section. $P\angle\varphi$ is used to evaluate the faults in the ADC, which will be illustrated later on.

3 The DUT and Fault Injection

An industrial 12-bit 80 Ms/s pipelined ADC is selected as the target device to validate our method. It is integrated into the analogue qualification vehicle (Aqua), which is fabricated by NXP semiconductors. The Aqua chip is a combined analogue test chip including several analogue blocks. It is used for silicon qualification of the analogue IPs, which also includes this 12-bit pipelined ADC.

Table 3 The setup of the input pulse signal for simulation

	Input frequency (MHz)	Duty cycle (%)	Rise or fall time (ns)	Number of samples
pulse 1	1.8	50	100	4096
pulse 2	1.8	50	100	16384

The architecture of this 12-bit ADC is shown in Fig. 6. It consists of ten stages. The basic architecture of each stage is identical, which is denoted by the dashed line in Fig. 6. Its major parts are a residue amplifier, an analogue adder, an ADC and a DAC.

For the simulation, this 12-bit pipelined ADC is modeled at the behavioural level using Labview. In the Labview model of the 12-bit pipelined ADC, there are several key parameters that can affect the performance of the ADC:

- The reference voltages of the comparators in the flash ADC of each sub-stage
- The values of the capacitors in the MDAC of each sub-stage
- The gain of the residue amplifier in the MDAC of each sub-stage

In the measurements, there is no faulty device available to validate our methods. As result, the faulty devices can only emulated by the fault-free devices. Usually, there are a lot of ways to realize this. However, concerning the matching of the simulations and the measurements, the way of emulation of the faulty devices must be the same or related to each other between the simulation and the measurement. Because of the limited accessibility to the ADC in the Aqua chip, a change of the supply voltage is the simplest way to realize it. As described before, there are three key parameters in the Labview model but only the gain of each sub-stage is related to the supply voltage [12]. As result, only the gain fault of the residue amplifier is injected into the

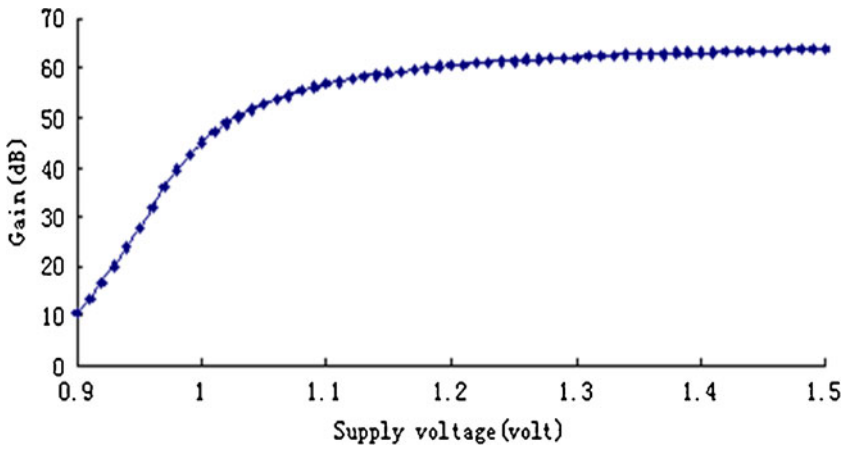

Fig. 7 Gain vs. supply voltage of the cascade opamp with gain boosted

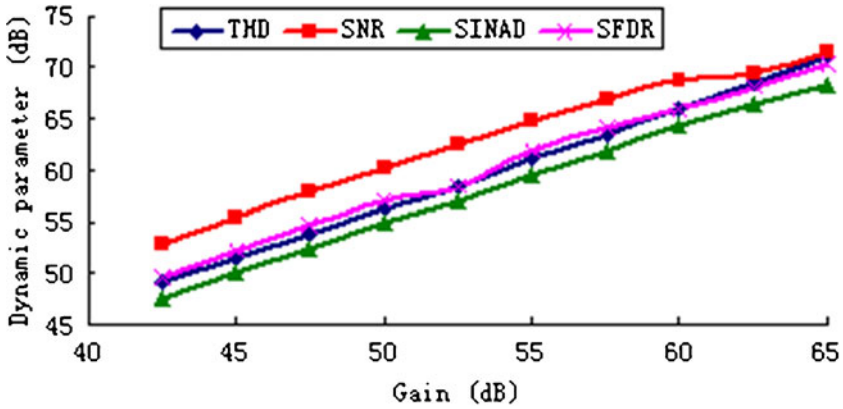

Fig. 8 The conventional dynamic parameters vs. the gain of the ADC in the Labview model

Labview model to emulate the change of the supply voltage in the measurement.

In order to show the relationship between the gain and the supply voltage, a simulation on a transistor-level design of a normal folded cascode Opamp with gain boosted has carried out [14]. The simulation results are shown in Fig. 7. One can observe that as the supply voltage decreases from 1.5 V till 1.1 V, the gain of the amplifier decreases slowly. If the supply voltage decreases below 1.1 V, which is the lowest supply voltage required for the amplifier, the gain of the amplifier drops very fast.

4 Simulations and Their Analysis

In order to validate our method, the simulation is carried out on the Labview model of the 12-bit pipelined ADC. The settings of the input pulse-wave stimuli are shown as in Table 3. The rising and falling edges of the pulse signal are modeled with 7-bit linearity as suggested in [7]:

$$x(t) = v_{os} + \eta\left[t + 0.04 * \left(t^2 - t\right)\right] + n(t) \quad (9)$$

,where v_{os} is the offset voltage, η is the slope and *n(t)* represents the noise. The part $0.04 * (t^2 - t)$ corresponds to the 7-bit nonlinearity property of the edges. For the entire pulse signal, a Gaussian white noise of 3LSB standard deviation has been added. Two different pulse signals are applied respectively. There is a larger number of samples of *pulse 2*.

In order to validate our methods, 10 different values of the gain of the residue amplifiers of the ADC are selected, which decrease from 65 dB to 42.5 dB. Figure 8 shows the Labview simulation results of the conventional dynamic parameters when the gain of every sub-stage of the pipelined ADC decreases. In Fig. 8, the dynamic performance degrades as the gain decreases. According to the specification of the 12-bit pipelined ADC, the fault-free range of the THD, SNR, SINAD and SFDR are 65 dB, 62 dB, 60 dB and 62 dB respectively. As a result, one can observe that the faulty ADCs are the ones with the gain of the residue amplifiers below 60 dB. Otherwise, the ADCs are fault-free. Here the ADCs are selected as the golden devices if the gain of the residue amplifiers is 60 dB, 62.5 dB and 65 dB respectively.

The simulation results of *P_am* and the $P\angle\varphi$ are shown in Figs. 9 and 10. In these two figures, the x-axis denotes the values of the gain of each sub-stage of the ADC and the y-axis denotes the results of the *P_am* or the $P\angle\varphi$. One can observe that as the gain decrease from 60 dB to 42.5 dB, the values of the *P_am* increases obviously. In this case, it matches the trend of the curve in Fig. 8. It proves that the *P_am* can reflect the faults in the ADC as do conventional dynamic parameters. Comparing the results obtained by *pulse 1* and *pulse 2*, one can also see that the slope of the curve is steeper when the

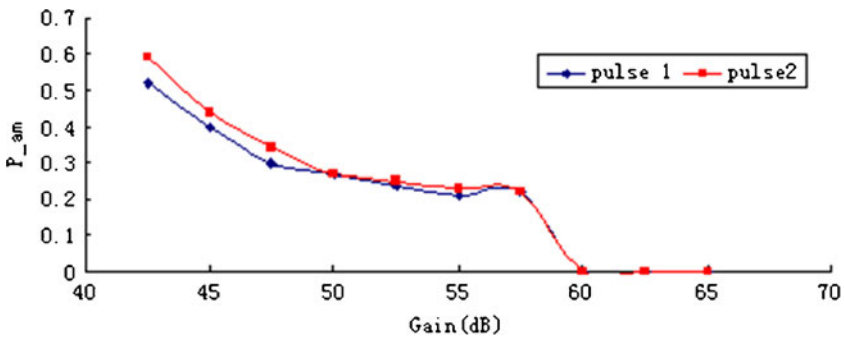

Fig. 9 *P_am* vs. the gain of the Labview model of the ADC

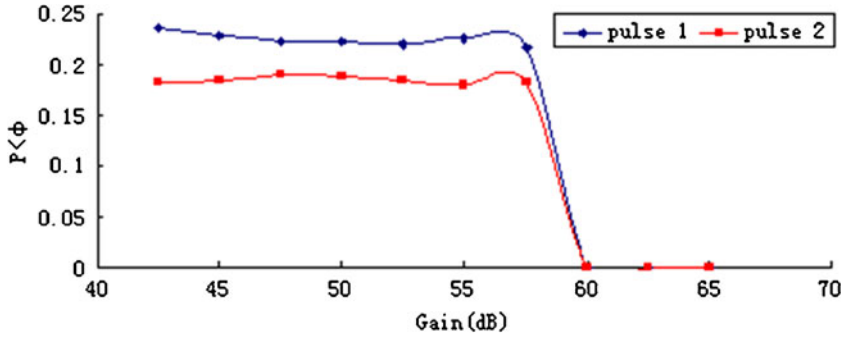

Fig. 10 $P\angle\varphi$ vs. the gain of the Labview model of the ADC

number of samples increases. It means the *P_am* becomes more sensitive to the faults.

In Fig. 10, one can observe that if the gain decreases from 60 dB to 57.5 dB, the $P\angle\varphi$ increases. However, if the gain changes from 57.5 dB to 42.5 dB, the curve of $P\angle\varphi$ becomes very flat. Hence, the algorithm of the comparison of angles cannot reflect the faults in the 12-bit pipelined ADC in a sensitive way.

From the Labview simulation results, one can see that the *P_am* can reflect the gain faults of the residue amplifier of the ADC in a similar way as the conventional dynamic parameters. As the samples of the input pulse signal increase, the *P_am* parameter can detect the faults in a more sensitive way. In contrast, the $P\angle\varphi$ cannot detect the faults in a sensitive way. However, in our previous work [11], the simulation results of a 6-bit flash ADC show that the $P\angle\varphi$ can detect as many faults as the *P_am*. Moreover, the $P\angle\varphi$ is more robust to the jitter and rise-and-fall-times variation of the input pulse-wave stimulus. As there is no corresponding 6-bit flash ADC available for measurement, we can not prove it with measurement results. As a result, we can only conclude that for the *P_am* can test 12-bit pipelined ADC better than the $P\angle\varphi$. However, for other types of ADCs, like flash ADC, the $P\angle\varphi$ has the potential to test the faults better than the *P_am*.

5 Measurement Setup and Results of a 12-Bit Pipelined ADC

For validating our algorithms, a 12-bit pipelined ADC in the NXP Aqua chip has been selected as the target device for the measurements. In order to investigate the robustness of the method, five different pulse signals are applied to the device respectively; they have different rise and fall times or number of samples. The parameters of the settings of these pulse signals are listed in Table 4.

As discussed in section 3, the faulty devices are emulated by changing the supply voltage level. Figure 11 shows the conventional dynamic parameters with different voltage levels. One can see that the curves of the dynamic parameters are relatively flat at from 0.99 V to 1.3 V. After 0.99 V, the values of the dynamic parameters drop very fast. As the supply voltage in the specification of the ADC ranges from 1.1 V to 1.3 V, the fault-free ranges of all the dynamic parameters are defined as the measurement values by operating the ADC from 1.1 V to 1.3 V. To emulate the collection of golden devices, the ADC operating at the voltage levels between 1.1 V and 1.3 V are used as golden devices.

In the real measurements, the output of each measurement cannot be synchronized. It means the reorganized output waveforms are not in the same phase, which will result in the incorrect calculation of *P_am* and $P\angle\varphi$. In this case, we just select the lowest level as the starting point of each reorganized waveform for the calculation of the signature results. This selection does not need to be very accurate.

Figures 12 and 13 show the measurement results of *P_am* and $P\angle\varphi$ respectively. The x-axis denotes the level of the supply voltage while the y-axis denotes the values of the *P_am* or the $P\angle\varphi$.

One can observe that if the supply voltage drops below 1.1 V, the values of the *P_am* become increasingly larger. When it drops around 0.98 V, the slope of the curve becomes steeper. The *P_am* shows a similar trend as the dynamic specifications with the variation of the supply voltage. As result, the signature *P_am* is as sensitive as the conventional dynamic parameters when detecting the faults of the ADC.

Comparing the curves of the *P_am* obtained with different pulse wave input stimuli in Fig. 12, they are quite close to each other, especially the part where the supply voltage is

Table 4 The settings of the pulse-wave stimuli in the measurement of the 12-bit pipelined ADC

	Input frequency (MHz)	Duty cycle (%)	Rise or fall time (ns)	Number of samples
Pulse 1	1.8	50	100	4096
Pulse 2	1.8	50	100	16384
Pulse 3	1.8	50	200	16384
Pulse 4	1.8	50	200	32768

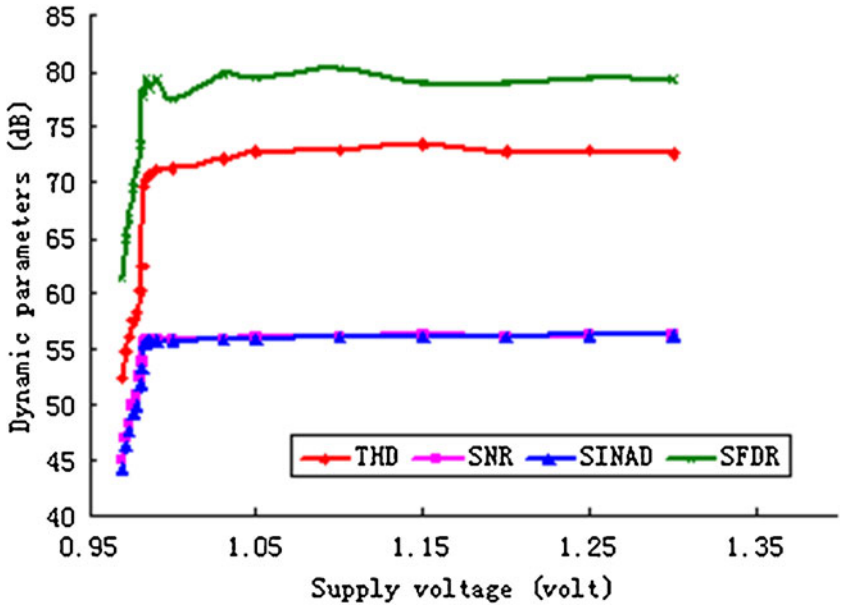

Fig. 11 Measured dynamic parameters of the 12-bit pipelined ADC vs. supply voltage

below 0.98 V. This means that the signature *P_am* is very robust with regard to the rise and fall edges and the number of samples of the pulse-wave input stimulus.

The measurement results of the $P\angle\varphi$ are shown in Fig. 13. If the voltage drops from 1.1 V to 1.05 V, $P\angle\varphi$ increases. However, as the voltage continues decreasing, the trend of the $P\angle\varphi$ becomes unstable. Therefore, it can be concluded that $P\angle\varphi$ can not detect the faults as sensitively as the dynamic parameters.

From the measurement results, one can see that the *P_am* can reflect the faults as the conventional dynamic parameters do. However, the trend of the $P\angle\varphi$ is unstable, which means it cannot reflect the faults as sensitive as the *P_am.* Although the rising and falling edges and the number of samples of the five input pulse signals are very different from each other, the *P_am* obtained by them are still relatively close. As result, the *P_am* is very robust to these settings of the input signal.

6 Comparison between Our Proposed Method and Conventional Testing Method

6.1 Input Test Stimulus

In the conventional specification test of an ADC, a high quality analogue ramp or sine wave signal is required, which is expensive to generate either on-chip or off-chip for the multi-site test environment. However, in the proposed testing method, an adapted pulse signal, which is easily to generate in a platform-based design, is exploited as the test stimulus. Obviously, in the case of an ADC integrated into a platform-

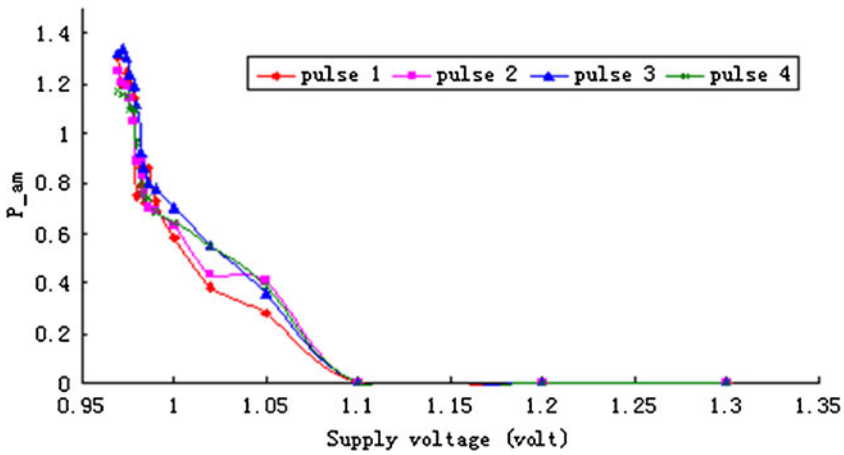

Fig. 12 Measured *P_am* of the 12-bit pipelined ADC vs. supply voltage

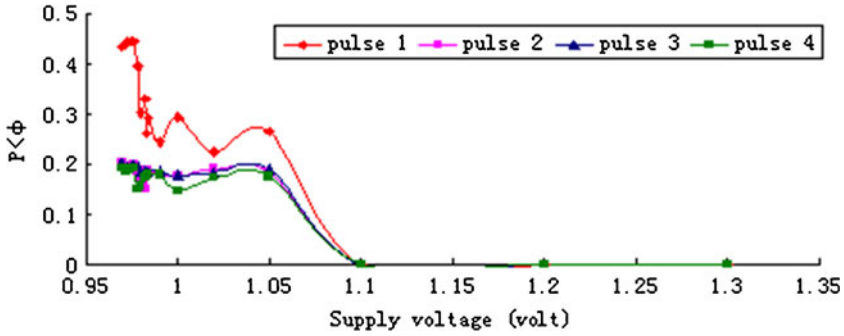

Fig. 13 Measured $P\angle\varphi$ of the 12-bit pipelined ADC vs. supply voltage

based design, the proposed method is less expensive and more simple for the multi-site test of the ADC.

6.2 ADC Output Data Post-processing

The FFT analysis and histogram method are applied to calculate the dynamic and static parameters respectively in the specification test. They are complicated and time consuming. However, the proposed algorithms only do a simple calculation based on the time domain output result. If we carry out the MatLab programs of the FFT analysis and the proposed algorithms on the same computer, the time of computation is 0.076 s and 0.01 s respectively. As a result, it can save more time, data processing power and memory.

6.3 Testing Result

The accurate specification results can be tested by using the conventional ADC test. The proposed method can only obtain a signature result to filter out most of the faulty devices. However, from the previous discussion, it is proposed as a quick and simple pre-test suitable to implement in a multi-site environment. After this pre-test, most of the faulty devices are discarded and only the devices, which pass the pre-test, have to take the complicated and time-costly specification test. If the *yield* of the chips is moderate, it can reduce the production test time and cost significantly.

6.4 Test Time

The total test time of the conventional ADC test is defined as:

$$T_c = t_{s\_c} * \frac{N_{DUT}}{s\_c} \tag{10}$$

, where t_{s_c} denotes the test time of conventional test for testing s_c sites, N_{DUT} denotes the total number of DUTs.

The total test time of the ADC test with the proposed pre-test can be defined as:

$$T_n = t_{s\_p} * \frac{N_{DUT}}{s\_p} + t_{s\_c} * \left(\frac{N_{DUT} - N_f}{s\_c} \right) \tag{11}$$

, where t_{s_p} denotes the time of pre-test for testing s_p sites, $N_{fault\text{-}free}$ denotes the number of DUTs passed by the pre-test. The *yield* can be defined as:

$$yield = \frac{N_{fault-free}}{N_{DUT}} \tag{12}$$

The ratio between the total test time with and without pre-test can be calculated as:

$$\frac{T_n}{T_c} = \frac{t_{s\_p}}{t_{s\_c}} * \frac{s\_c}{s\_p} + yield \tag{13}$$

If we assume t_{s_p}/t_{s_c}=0.01/0.076 as obtained in section 5.2, the relationship between T_n/T_c and *yield* is shown in Fig. 14. The x-axis denotes the yield while the y-axis denotes T_n/T_c. As s_c/s_p changes from 0.1 to 1, the production test time can be reduced by 13 %. It can be observed that the proposed method can reduce the production test time increasingly as the yield becomes lower. When the devices are fabricated with a not fully matured process, the yield can be lower to 90 %~95 %.

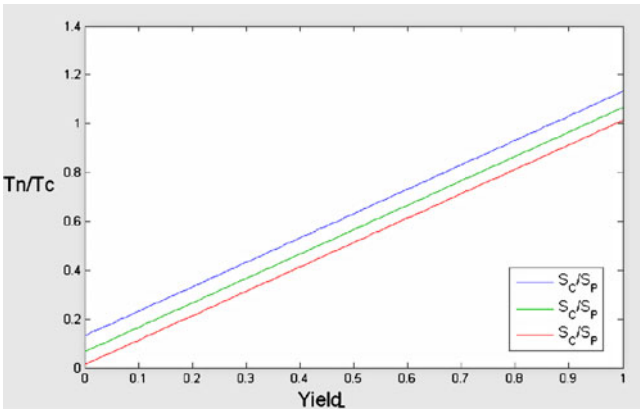

Fig. 14 The *yield* vs. T_n/T_c with s_c/s_p as the parameter

In this case, the proposed test method can help to reduce the production time. However, for a matured process, the yield is higher than 99 %, this method can not reduce production time.

7 Conclusion

In this work, an ADC pre-test based on two novel algorithms has been proposed. In these two algorithms, the most simple digital wave form, a pulse signal, is taken as the test stimulus as it is easy to generate in a platform-based design, in which more and more ADCs are integrated nowadays. Through a simple and fast data process of the algorithms, a signature result, out-of-amplitude-range percentage or out-of-angle-range-percentage, can be obtained to decide if the DUTs pass or fail the test. This can be easily accomplished on chip. The basic concept of these two algorithms is evaluating the faults in the ADCs by comparing the similarity between the outputs of golden devices and DUTs in the time domain. The similarity between them is by calculating the deviation of amplitude or angle of the ADC outputs. An industrial 12-bit pipelined ADC has been used to verify these two algorithms in both simulations and measurements. It shows that compared with the conventional dynamic parameters, the P_am can detect the faults in a similar sensitive way. However, the $P\angle\varphi$ cannot. Moreover, the P_am is very robust to the edges and number of samples of the input stimulus. However, we can conclude that the P_am can detect the faults better than the $P\angle\varphi$ for the 12-bit pipelined ADC. As the input test signal is easy to generate on-chip, these two algorithms are very suitable for multi-site test. Based on this precondition, we proposed to exploit either of them as a pre-test to filter out most of the faulty devices. The complicated and time consuming specification test is only necessary to carry out on the fault-free devices. In this way, it will help to reduce the production test time and cost of ADCs significantly, especially when the devices are fabricated with a not fully matured process.

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