New Statistical Timing Analysis Method Considering Process Variations and Crosstalk

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I. ABSTRACT (SESSION 2)

A. Statistical Gate Delay

Static Timing Analysis (STA) tools are widely used for efficient timing checks on large chips. In early times, the nonlinear delay model (NLDM) was widely used for STA. As technology downscaled into ultra-deep sub-micron region, noise and coupling considerations require advanced gate modeling for STA. Croix and Wong proposed a current source drive models (CSDM) which model every gate by a voltage-dependent current source and capacitor [1]. However, some effects, such as internal charge sharing and multiple input simultaneous switching (MISS) can not be captured by such a simple model. These issues are addressed by transistor-level gate models which achieve higher accuracy [2], [3].

If the process variations are not considered, those gate models achieve high accuracy for STA. However, the down-scaling of technology brings a significant increase in the device and interconnect manufacturing process variations, such as length (L_{eff}), threshold voltage (V_{th}), wire width (W_w) and wire thickness (T_w). Therefore, there is a need for advanced analysis tools which can handle variability caused by imperfect manufacturing processes. In order to capture the impact of process variations on gate behavior, statistical STA (SSTA) becomes more and more attractive.

Most published SSTA methods can be called function-based SSTA since the gate delay is modeled as a linear or non-linear function of process variations and the coefficients are characterized and stored in look-up tables with entries of S_{in} and C_{eff}. This modeling approach is similar to the NLDM concept thus has the accuracy limitations same as NLDM. Not considering the statistical S_{in} and C_{eff} can result in 30% delay errors and even worse for bigger circuits [4]. The function-based delay representation is entirely based on non-physical or empirical models, which is the major source of inaccuracy [5]. In order to increase accuracy, CSDMs have be extended for SSTA in [4]–[6]. However, these methods are just verified in several simple single gates, and the correlations among input signals and between input signal and delay are not considered.

To gain even higher accuracy than the above CSDM methods, and to be able to see the important effects such as MISS, we propose a statistical timing analysis solution based on transistor level gate models [3] to provide the variational voltage waveforms [7]. The gate models are constructed from CSDM-like transistor models. Due to the process variations, the nodal analysis equation of every gate becomes a random nonlinear differential equation. In our algorithm, during the analysis of every gate, the random nonlinear differential algebraic equation is linearized by first-order Taylor expansion. After linearization, the equation is divided into two parts: i) $F(\dot{v_s}, v_s, t, p_0) = 0$, an ordinary differential equation (ODE) equation for nominal output where v_s is the nominal value of state variables like voltages and p_0 is the nominal value of process parameters; ii) $\mathbf{C}(v_s)\dot{y}(t) = \mathbf{E}(v_s)y(t) + \mathbf{F}(v_s)\xi$, a random differential equation (RDE) for voltage variations $y(t)$, where $\mathbf{C}$, $\mathbf{E}$ and $\mathbf{F}$ are coefficient matrices [7]. The first equation can be solved by existing methods [2], [3]. According to the RDE theory, the second equation can be solved by using a normal ODE solver [7], [8]. Based on the solution of these two equations, the voltage at every time point is represented by $\hat{v(t)} = v_s(t) + \mathbf{\Psi}(v_s, t)\xi$, where $v_s(t)$ and $\mathbf{\Psi}(v_s, t)$ are obtained from equation i) and ii) respectively and ξ is the process variation. The mean, variance and covariance of voltages are computed after obtaining $v_s(t)$ and $\mathbf{\Psi}(v_s, t)$.

For timing analysis, the problem of interest is to compute the moments of arrival time, gate delay or in general crossing time. The discretized probability density function (pdf) of the crossing time of interest (e.g. 50% crossing time for delay calculation) is calculated based on the statistical moments of voltages. Therefore, the moments (mean, variance and skewness) of crossing time can be obtained. The variational waveform and its discrete pdf computed using our algorithm is illustrated in [7], [8].

The proposed solution has the following features:

- The variational waveform, which models several varying crossing times, is calculated and propagated through circuits;
- In the RDE-based statistical gate analysis, all input signals are considered together and calculated directly, thus fundamentally addressing MISS in statistical timing analysis;
- As we use a common format for waveforms and elements in gate models, the correlations among input signals and between input signal and delay are preserved during pdf computation;
- Arbitrary process variation distributions, Gaussian or non-Gaussian, can both be handled in the method;
- The voltage sensitivity in the RDE equation is calculated efficiently by using fast linear algebraic equation solvers.

B. Statistical Interconnect Delay with Crosstalk

Existing timing analysis methods analyze the gate delay and interconnect delay separately. Interconnect delay is affected by process variations in a complex way and the ratio of process variations with respect to their corresponding nominal values is increasing. Therefore, the impact of process variations (PVs) on interconnect delay must also be taken into account for accurate SSTA. Besides process variations, the effect of crosstalk on delay increases with each new technology generation. Crosstalk may increase path delay up to 30%, making it the biggest variation component within a die [9]. Therefore, accurately estimating interconnect delay distribution with crosstalk effects is an absolute necessity for timing analysis.

The interconnect delay distribution in the presence of crosstalk effects strongly depends on the arrival time difference (input skew). According to [10], the interconnect delay moments (μ_{total}, σ^2_{total}) can be calculated as follows.

$$\mu_{total} = \mu_{sk} + \mu_{pv}(\mu_s) - D_0 \quad (1)$$

$$\sigma^2_{total} = \sigma^2_{sk} + \sigma^2_{pv}(\mu_s) \quad (2)$$

where μ_{sk}, σ^2_{sk} and μ_{pv}, σ^2_{pv} are moments of input skew induced (SK-induced) and process variation induced (PV-induced) interconnect delay, respectively. μ_s denotes the mean of input skew.

SK-induced interconnect delay. After performing simulation on different coupled wire types, we observe that the delay-change-curve (DCC) can be modeled as a piecewise linear function with respect to the input skew [11]. Therefore, in contrast to [10], we approximate delay as a piecewise linear function of input skew as shown in Fig. 1. Higher accuracy can be obtained by more segments without introducing more complexity for calculation.

PV-induced interconnect delay. The mean and variance of PV-induced interconnect delay also strongly depend on the mean of input skew. Even though the influence of input skew and process variations on interconnect delay can be considered independent, the PV-induced interconnect delay calculation must take input skew (μ_s) into account in nanometer technologies. The empirical method [11] or analytical methods [12] can be used.

The proposed solution has the following features:

- The mean and variance of SK-induced interconnect delay is evaluated analytically in closed form in constant time;
- Both Gaussian and non-Gaussian input skew can be handled;
- PV-induced interconnect delay is calculated considering coupling effects;
- The total interconnect delay moments are computed from SK- and PV-induced interconnect delay;
- The DCC characterization only needs 15-25 samples which is more efficient than Monte Carlo simulations.

C. Experiment Results

The effectiveness and accuracy of the proposed gate delay calculation method was evaluated on some commonly used

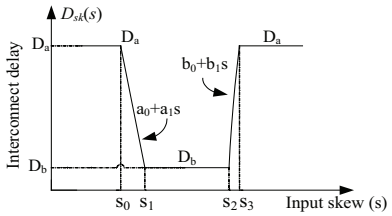

Fig. 1. Delay change curve (DCC) model for SK-induced interconnect delay

standard cells and ISCAS85 benchmark circuits using GVT library of PTM 45nm technology. For a full range of input skew and load capacitance, the deterministic delay and slew calculation on different cells both have average errors within 1%. This shows the high accuracy of the transistor-level gate modeling. The L_{eff} and V_{th} are chosen as the representative process variables, which both have 3σ equal to 20% of the mean value with different correlation coefficients. The proposed statistical timing analysis method is evaluated in C17, Adder, C432 and C499. The maximum μ and σ errors are 1.15% and 2.97% which indicates the high accuracy of our method. Compared to Spectre MC runs, our method achieves $712\times$ speed-up on average [7].

The interconnect delay calculation method is evaluated in different coupled wires: local, intermediate and global wires, driven by both strong and weak drivers. We tried the full range of input skew mean values and capacitances. The W_w and T_w are chosen as process variations of wires. The maximum delay μ and σ errors are 0.75% and 3.53%. It should be noted that the results are even better for long global wires (the maximum delay μ and σ errors are 0.30% and 0.59% for $500\mu m$ coupled global wires with $100ps$ input transition time [11]).

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