

# Statistically aware buffer planning

Giuseppe S. Garcea, Nick P. van der Meijs  
Kees-Jan van der Kolk  
Delft University of Technology  
Faculty of EEMCS, The Netherlands  
giuseppe@cas.et.tudelft.nl

Ralph H. J. M. Otten  
Eindhoven University of Technology  
Faculty of EE, The Netherlands

## Abstract

*In this paper, we will develop an analytic approach to estimate the statistical properties (mean and variance) of the performance of a uniformly buffered global IC interconnect, based on the mean and (co)variance of the appropriate design and technology parameters. Compared to other approaches, such as Monte Carlo based design optimization loop and provide a better insight in the factors involved. The model that we use is generic, but in this paper we assume a set of synthetic (not based on actual process data) but realistically large values for the variability of the input parameters. Under these assumptions, it follows that solutions for the area/power/performance tradeoff that are optimal in a deterministic setting, might suffer from excessive variability, potentially leading to a yield problem.*

## 1. Modelling performance variability

The approach proposed [5] uses the 2<sup>nd</sup> order Taylor expansion of a function  $\phi$ , which represents a generic quality figure. This is a non-linear function of the vector of random variables  $P = (p_1, p_2, \dots, p_n)$ . The nominal value of the parameters is denoted by  $P^0 = (p_1^0, p_2^0, \dots, p_n^0)$ . Details are presented in [6].

According to [5], the total variance for the Taylor expansion of  $\phi$  is:

$$\sigma^2(\phi(P)) = \sum_i \left( \frac{\partial \phi}{\partial p_i} \right)^2 \sigma_{p_i}^2 + 2 \sum_{i>j} \frac{\partial \phi}{\partial p_i} \frac{\partial \phi}{\partial p_j} \text{cov}(p_i, p_j) \quad (1)$$

In this contribution we typically present the results in normalized form as the ratio between the standard deviation (square root of the variance) and the expected value. The notation  $\sigma_n(\phi(P))$  will denote the following ratio:

$$\sigma_n(\phi(P)) = \frac{\sqrt{\sigma^2(\phi(P))}}{E(\phi(P))} \quad (2)$$

where  $E(\phi(P))$  is the expected value modelled as in [6]. We will focus on the effect of variability on the performance,

which is defined as the signal velocity propagation [2]. This variability estimation can drive a new approach to uniform buffer planning for point to point connections.

## 2. Impact of interconnect variability

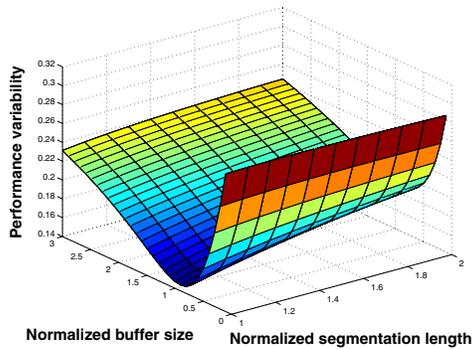
We employ uniform buffer planning as in [4]. The output of the model is buffer size and buffer distance. we normalize these dimensions with respect to those for maximum performance as obtained by Bakoglu (see also [4]). Performance is measured as  $v^{-1}$ , the inverse of the propagation speed. The input of the model is a set of parameters relating the interconnect and device properties. We assume that they are (almost) uncorrelated, if not we rewrite them in terms of more primitive parameters with low enough correlation. This simplifies the analytic treatment. However, correlation among these low level parameters can be included if necessary, by including the appropriate covariance term in (1) [5].

We use typical parameters for a 0.18 $\mu\text{m}$  technology. We assume that all parameters have the same normalized standard deviation  $\sigma_n = 20\%$ . It is important to stress that this assumption is made only in order to give a quantitative example, but the framework that has been created can be used for each standard deviation derived from realistic process measurements. See [3] for our online version of the model that allows to adjust the different parameters of the model.

The total contribution of the interconnect variations on the standard deviation of  $v^{-1}$  is presented in Figure 1.

The standard deviation appears to be only a weak function of the buffer distance, which is furthermore decreasing for shorter lengths.

The dependence of the standard deviation on the buffer size seems to be less obvious. The performance variability is minimized in this example for the buffer size of 0.8 $w_{bakoglu}$ . It must be noted that large buffers of size  $w_b > w_{bakoglu}$  (normalized buffer sizes  $> 1$ ) are never advantageous when variability is disregarded [4]. This analysis shows that also when interconnect variability is considered, such large buffers only reduce the predictability.

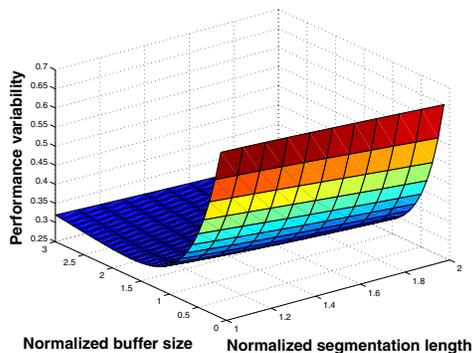


**Figure 1. Total impact of interconnect variability on performance**

The useful range of  $w_b$  thus seems to remain restricted to  $w_b < w_{bakoglu}$ . However, for really small buffer sizes the performance variability might become unacceptably large.

### 3. Impact of simultaneous device and interconnect variability

We can evaluate the impact on the inverse of velocity of the device and interconnect variability together and plot the standard deviations in the design parameter space composed by normalized buffer size and buffer distance. The result is shown in Figure 2.



**Figure 2. Total effect of variability**

This figure still shows a weak dependence of the variability on the length of the segment. This is desirable because by placing a suboptimal number of buffers on the global wire, the variability of  $v^{-1}$  is only marginally affected. Performance variability then seems to depend mainly on the value of the buffer size. In particular for really small buffer sizes, the variability can become really large. We can estimate at

least for this example that for  $0.5 < w_b/w_{bakoglu} < 1.5$  the increased standard deviation actually remains below 10%, but for still smaller sizes the standard deviation is increasing very rapidly. Thus, Figure 2 indicates that small buffer sizes are very unfavorable from a predictability point of view. This actually could augment the results from [4].

### 4. Conclusion

We have developed a general analytic approach for estimation of the statistical properties of a uniformly buffered uniform RC line for global interconnect. The model takes as input the mean and (co)variance of the controllable design and technology parameters. It was concluded that a fully deterministic model to tune the buffer size and segment length might cause yield problems because of excessive variability.

No inductive effects nor correlation among the input parameters have been assumed in this work. However, these are non-essential simplifications and can be alleviated when necessary for a particular purpose. The only requirement is that this model is analytic, such that the necessary derivatives exist to perform the steps of Section 1. Of course, this approach loses its numerical validity when the models are too rough or when the variability becomes so large that the Taylor expansion becomes inaccurate. However, in the range of validity of this model, its advantages include a possibly tight and fast design optimization loop and effective 'what-if' analysis. The validation of the proposed model with Monte Carlo based approach can be found on the web [3].

Furthermore, this approach can be extended to directly give design-for-yield solutions. For example, we can find the minimum buffer area for a certain performance under yield constraints.

### References

- [1] M. Orshansky, C. Spanos and Hu Chenming. *Circuit performance variability decomposition*. in Proc. of the 4th International Workshop on Statistical Metrology (IWSM), pp. 10-13, Jun. 1999.
- [2] R.H.J.M. Otten and R.K. Brayton. *Planning for performance*. in Proc. 35th Annual Design Automation Conf., pp. 122-127, Jun. 1998.
- [3] web site: <http://www.space.tudelft.nl/warp>
- [4] G.S. Garcea, N.P. van der Meijs and R.H.J.M. Otten. *Simultaneous analytic area and power optimization for repeater insertion*. in Proc. International Conf. on Computer Aided Design, Nov. 2003.
- [5] A.V. Metcalfe. *Statistics in Engineering, a practical approach*. Reading, Chapman and Hall, 1994.
- [6] G.S. Garcea, N.P. van der Meijs and R.H.J.M. Otten. *Buffer Planning for Global Wires under Statistical Process Variations*. in Proc. ProRISC, Nov., 2003. .