MONOLITHIC INTEGRATION OF LEDs AND SILICON PHOTOMULTIPLIERS IN STANDARD CMOS TECHNOLOGY FOR CONSUMER APPLICATIONS

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Abstract– An optical emitter and detector system based on an all-digital approach is presented for use in human-computer interfaces, whereas in this paper we focus on an optical joystick application. The emitter consists of 16x16 array of silicon light-emitting avalanche photodiodes biased above breakdown. Detection is performed by four digital silicon-photomultipliers (SiPMs) in a central-symmetry arrangement. The chip allows click and angle detection based on the pressure and tilt applied to a joystick knob coupled to a micro-mirror.

I. INTRODUCTION

Currently, there is an increasing interest in conjugating optical functionality to integrated circuits in native CMOS technologies. Direct integration of such optoelectronic devices into microelectronic circuitry with standard CMOS processing would effectively reduce manufacturing costs, increase yields, and decrease the bill-of-materials in many applications [1]. Furthermore, on-chip electronics can also implement highly complex signal processing functions and thus contribute to the realization of powerful sensor systems. In this paper a novel monolithic emitter-and-detector design fabricated in standard CMOS technology is presented for an optical joystick system.

II. OPTICAL JOYSTICK - CONCEPT

A joystick is an input device consisting of a stick that pivots on a base, and reports its angle and direction to the device it is controlling [2]. Fig. 1 shows the concept of the optical joystick; it comprises a light emitting diode (LED) and an array of four digital silicon photomultipliers (d-SiPMs). A d-SiPM is an array of SPADs whose outputs are digitally combined to perform single-photon counting on a large area. A mirror is mounted at the bottom of the joystick pole, so that different positions involve a different photodiode illumination. When the joystick is upright in the rest position, light from the LED is reflected by the mirror and shines a symmetric light circle onto the d-SiPMs, as shown in Fig. 2(a). When the joystick is tilted, the mirror follows the same motion and the light circle moves away from its center position, see Fig. 2(b), thus causing a photon-count differential between the d-SiPMs. When the joystick is pressed vertically, the received light intensity increases, and can be interpreted as a click signal. Due to the digital nature of the d-SiPMs, the X, Y, and click coding is done directly, without the use of A/D converters.

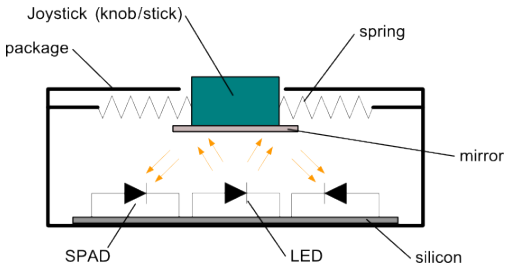


Fig. 1. Proposed optical joystick system. The device consists of light emitter LEDs and four d-SiPMs. A mirror is mounted at the bottom of the joystick knob, and is controlled with a spring.

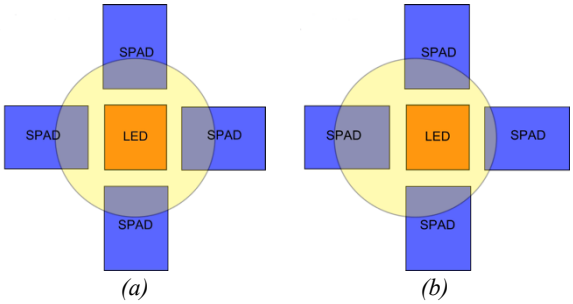


Fig. 2. Working principle of the proposed optical joystick system. The LED light is reflected by the mirror and shines a circle on the d-SiPMs. (a) An equally spread circle results from a joystick in neutral position. (b) The circle shifts more towards the left if the joystick is tilted more in the right direction. A click is captured by a uniform intensity increase.

III. CHIP ARCHITECTURE

Fig. 3 shows the block diagram of the system including the center LED and four d-SiPMs. Photon counting is performed with a simple digital counter. Additional digital logic is included on-chip to calculate angle and click information. Each d-SiPM consists of an array of 20x16 passively quenched SPADs with a 4µm diameter active area and a 19.5µm pitch. Individual SPADs can be disabled independently, allowing for hot pixels to be masked.

The d-SiPM is hierarchically organized as an array of 10x8 clusters of 2x2 SPAD pixels. The outputs of each SPAD in the cluster are combined into a single channel using

an OR gate, as shown in Fig. 4; this results in a spatial compression, since the four individual SPADs are acting as a single 4x larger one, with ¼ of dead time τ_D, assuming that the photon count is much lower than the inverse of the SPAD dead time. With larger fluxes, the pulses begin to overlap and the detected photon count reaches saturation and eventually decays to zero.

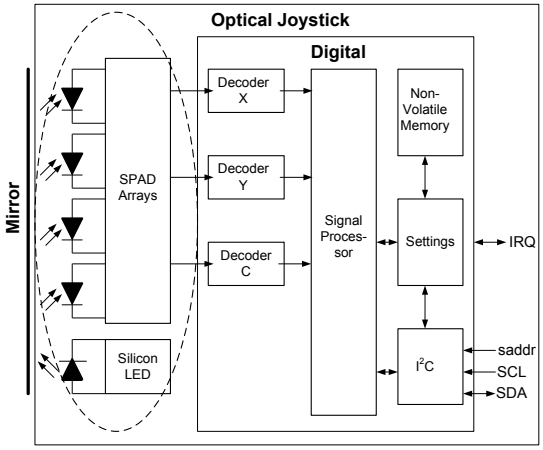


Fig. 3. Block diagram of the proposed system; it consists of a LED array in the center, four d-SiPMs, one for each direction (left, right, top, and bottom), and digital logic for control purposes.

To mitigate this effect, the pulses should be reduced to an infinitesimal width, approaching Dirac pulses; this technique is known as time compression. A good approximation of ideal time compression is achieved through a monostable circuit with variable pulse width [3]. The question is where to place the monostable, so as to achieve the best tradeoff between fill factor and photon count loss due to saturation. To investigate this tradeoff, we placed one monostable circuit at the output of each SPAD (see Fig. 4) and we varied the width of the pulses from 1 to 10ns for a range of photon flux values.

The overall detected photon count was found to be logarithmic, approximating linear behavior at low photon fluxes and asymptotically reaching $N/(e \cdot \tau_D)$ at high fluxes, N being the number of monostable circuits, before decaying to zero at very high photon fluxes. In case of active quenching, the factor e goes to 1 and the decay to zero occurs at infinite photon fluxes.

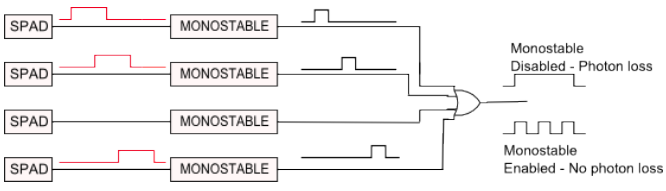


Fig. 4. Block diagram of the two compression schemes (spatial and temporal) working in tandem.

This behavior is consistent with theory, when it is assumed that photon arrivals are uniform in space and follow a Poisson distribution in time before their wave function collapses at the detector's surface [4].

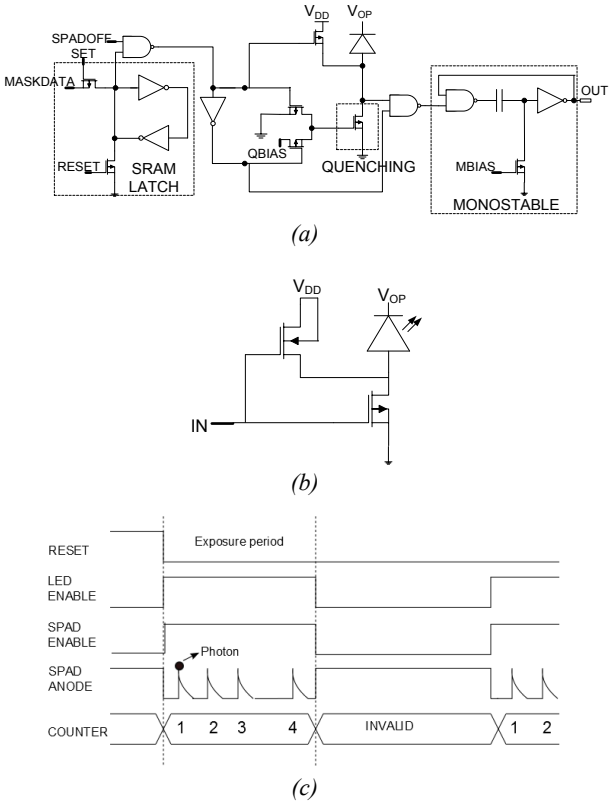


Fig. 5. Schematic diagram of a LED and a SPAD pixel. (a) SPAD pixel with passive quenching, 1-bit memory, and monostable pulse shaping circuit. (b) LED with a strong pull-down and clamp. (c) Timing diagram with both SPAD and LED enabled during the exposure period.

To improve fill factor, temporal compression can be restricted to clusters instead of individual SPADs. In our case, only 10x8=80 monostable circuits could be used, resulting in a photon count loss of less than 5% but a far higher fill factor and thus a net photon detection efficiency (PDE) gain. Each SPAD pixel consists of a photodiode, quenching circuitry, mask memory, monostable and some associated electronics.

The center LED array consists of 16x16 pixels with a 4µm diameter active area and a 20µm pitch. The LED emission is based on impact ionization, as opposed to bremsstrahlung as in [5]; though less efficient, it requires a smaller current for an emission that is sufficient for detection. The LED driver is an asymmetric inverter with a strong pull down NMOS for speed and current drive and a weak PMOS acting as a clamp. Each cluster consisting of 2x2 SPAD

pixels can be enabled independently, allowing a good tradeoff between light intensity and power consumption.

Fig. 5(a) and (b) show SPAD pixel and LED architectures, respectively. Fig. 5(c) shows the timing diagram, where both SPADs and LEDs are enabled only during the exposure period, to save power.

IV. Results

Fig. 6 shows a microphotograph of the chip, fabricated in 180nm standard CMOS technology. The total area is 1.7 x 1.5 mm^2.

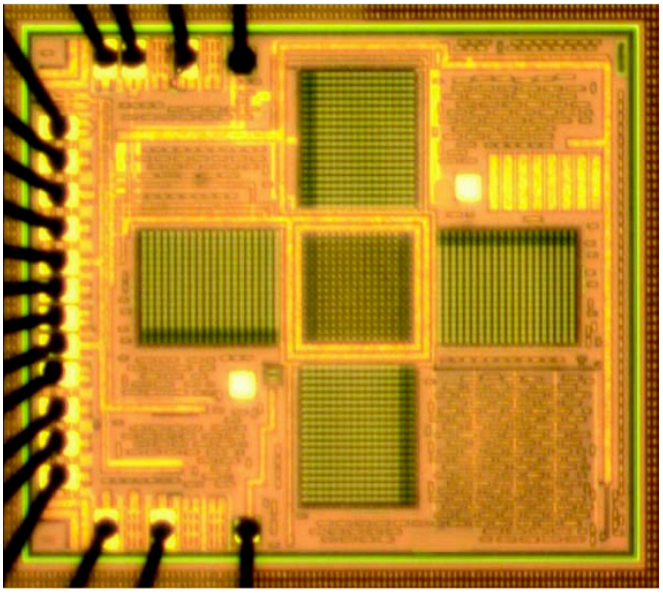


Fig.6. Photomicrograph of the optical joystick chip with the emitter array in the center and four d-SiPMs, one for each direction. Digital logic is included for hot pixel masking, control, and readout purposes.

Fig. 7 shows the dark count rate (DCR) cumulative probability distribution for an excess bias voltage of 2V at different temperatures. At room temperature, 9.5Hz is the median DCR of this chip, whereas the DCR per active area is 0.75Hz/mm^2. Also, the median DCR of the array reduces to around 2Hz at -40^{o}C. Fig. 8 shows the photon detection probability (PDP) as a function of wavelength. The measurements were performed at room temperature between 360nm and 800nm. The PDP is higher than 30% between 460nm to 560nm at 4V excess bias, with a peak of 43% at 480nm. Masking hot SPAD pixels, by turning off noisy SPADs, represents a tradeoff between PDE and DCR. Fig. 9 shows the evolution of DCR with various masking ratios and the consequent PDE variation at 3 different temperatures. For small masking DCR benefit is greatest and PDE reduction minimal. For larger masking levels, DCR improves negligibly, while PDE keeps on decreasing linearly.

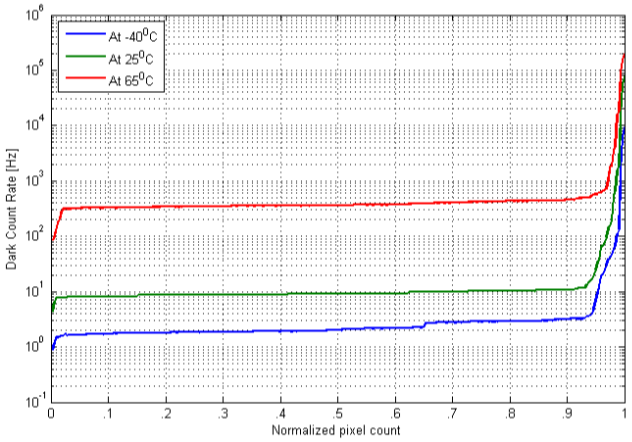


Fig. 7. Dark count rate (DCR) cumulative probability distribution for 2V excess bias at -40 ^{o}C, 25 ^{o}C, and 65 ^{o}C.

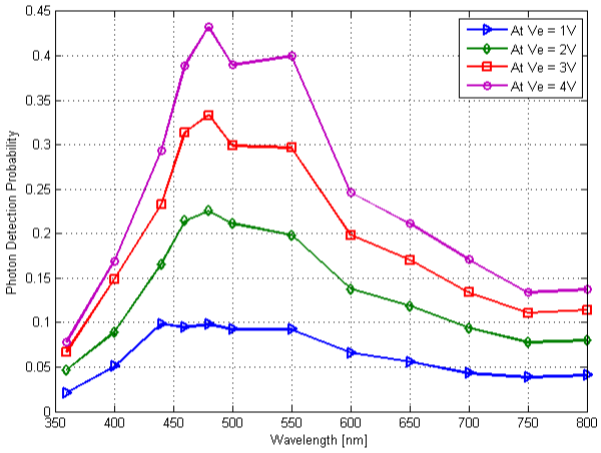


Fig. 8. Photon detection probability (PDP) as a function of wavelength for different excess bias voltages.

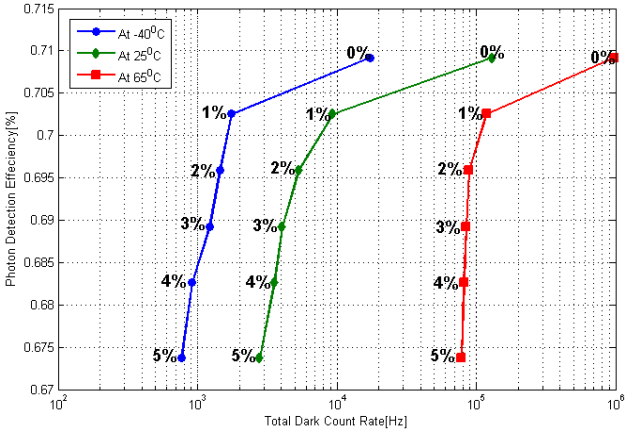
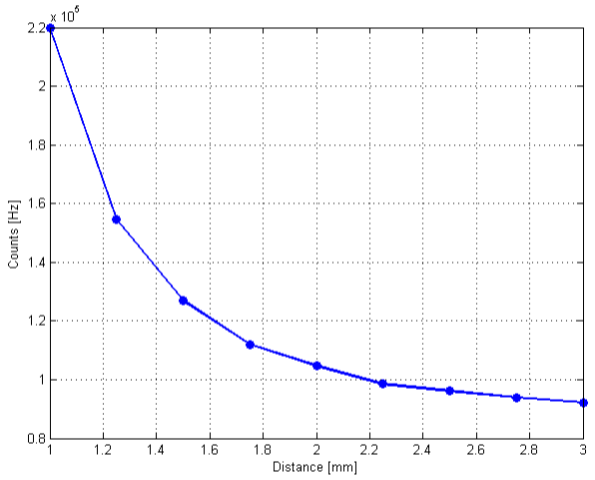
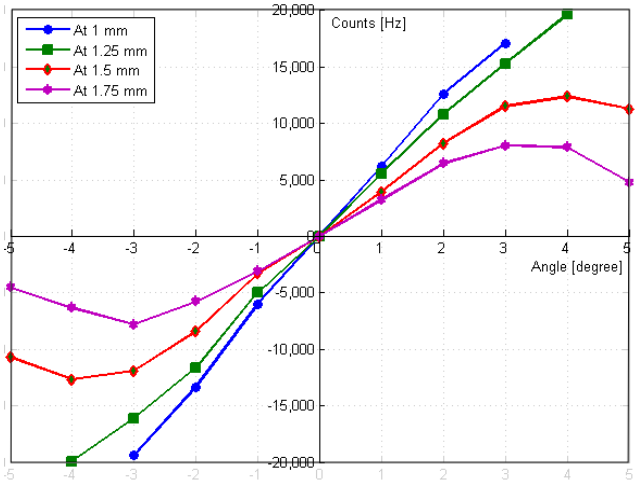


Fig. 9. Effect of masking on PDE and DCR. The measurement was performed at -40 ^{o}C, 25 ^{o}C and 65 ^{o}C.



(a)



(b)

Fig. 10. Optical joystick measurement for click and angle detection. (a) Click Detection – change in the measured light intensity with respect to the distance of the mirror from the chip. The light intensity decreases with distance. (b) Angle Detection – Measured count difference between top and bottom array as a function of mirror tilt for different distances. The count difference increases with the tilt until the light circle moves away from the chip.

Finally, the chip was tested for joystick functionality (click and angle detection) by mounting a mirror overhead. Fig. 10(a) shows the decrease in light intensity with the increase in distance between chip and mirror. Fig. 10(b) shows the angle measurement. Tab. 1 summarizes the measured data of the overall system.

V. Conclusions

An all-digital optical emitter / detector system was proposed and demonstrated for use in an optical joystick application. The emission and detection is performed through arrays of avalanche photodiodes operating in Geiger mode and arranged in central-symmetry. The system has the advantage of integrating light sources and detectors in a single CMOS chip, thereby reducing costs and improving yields. The chip allows click and angle detection based on the pressure and tilt applied to a joystick knob coupled to a micro-mirror.

Tab. 1. Performance summary of the chip.

Parameter	Value	Unit
LED Array size	16 x 16	pixels
LED Pixel size	20 x 20	μm^2
SPAD Array size	20 x 16	pixels
SPAD Pixel size	19 x 19	μm^2
Fill factor	3.5	%
Median DCR @ V_e=2V	9.5	Hz
PDP @ V_e=2V	23 @ 480nm	%
Crosstalk	< 0.01	%
Jitter (FWHM)	120	ps
Frame rate	10-100	fps
Chip Area	1.7 x 1.5	mm^2

Acknowledgement

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