Reduction of Fixed-Position Noise in Position-Sensitive Single-Photon Avalanche Diodes

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***Abstract*—By ignoring events originating in noisy areas of a position-sensitive single-photon avalanche diode (SPAD), reduction of noise from fixed-position defects is experimentally shown. Additional experimental results from a position-sensitive SPAD integrated in a high-voltage 0.35-μm technology are presented. An effect reducing the active area is described, quantified, and experimentally measured using multiple techniques, with an observed inactive distance of roughly 2 μm near the guard rings. The standard characterization results for multiple SPAD geometries are presented, along with the results of noise reduction in a single high-noise SPAD. Characterization results show a photon detection probability above 35%, a dark count rate density in the tens of Hz/μm^2, and a signal-to-noise ratio increase of 8 dB for a noisy diode in low light.**

***Index Terms*—Avalanche breakdown, semiconductor device noise, single-photon avalanche diodes.**

I. Introduction

SINGLE-PHOTON avalanche diodes (SPADs) have been proposed for use in hostile environments such as space or ultracold temperatures [1], [2]. Within these environments, fixed-position noise can be problematic, whether from traps created by ionizing radiation or defects introduced at fabrication time. This paper presents the realization of a technique to reduce noise from fixed-position defects in position-sensitive SPADs created in a CMOS technology [3]. The idea of using large position-sensitive avalanche diodes is also potentially interesting to fields such as positron emission tomography and fluorescence lifetime imaging microscopy systems, which require high-fill-factor high-spatial-resolution devices [4]–[6]. However, there are some drawbacks to position-sensitive avalanche diodes that use the voltage rise time to estimate the position. First, the sensitivity to the avalanche seed position is not uniform. This issue is further exacerbated by the similar rise times caused when an avalanche is triggered anywhere at the edge of a symmetric structure. Second, the ionization noise distorts the position resolution [7]. Third, some method to measure the rise time is required; it is not clear how to integrate circuitry with this functionality on chip, though chips with a time-to-digital converter (TDC) per SPAD have previously been reported [8].

In addition to experimental results from a position-sensitive SPAD in a CMOS technology, a comparison of the standard characterization of multiple geometries is shown, with the aim of characterizing an effect that distorts the measured geometries. Measuring the effect is necessary to match measurements from multiple geometries. The distortion, possibly caused by the type of guard ring used, is important to any field where SPADs are used, even if it only provides additional evidence that guard rings based on doped wells have poor performance compared to shallow-trench isolation (STI)-bound SPADs.

II. Device Overview

This section presents a custom IC created to study position sensitivity in SPADs [3]. The custom IC, which is named the multioperation SPAD array integrated circuit (MOSAIC), contains SPADs of four different geometries coupled to TDCs. Three of the four diode geometries contain p+ implants that are circular with diameters of 6, 12, or 24 μm, with the guard ring outside the p+ implant. In the figures that follow, these SPADs will be labeled by their p+ implant diameter. The chip also contains an SPAD with a pill-shaped geometry. This SPAD has a p+ implant of a 6×24 μm^2 rectangle capped by two semicircles, both with a radius of 3 μm. Different metal coverings of this pill-shaped structure are included on MOSAIC, including a completely open SPAD, a completely covered SPAD, an SPAD covered except for the edge, and an SPAD covered except for the middle. The four different SPAD geometries are shown in Fig. 1, along with the partially covered pill-shaped structures. While the active area is normally expected to match the p+ implant, evidence will imply that this is not the case.

As shown in Fig. 2, coupled to each SPAD are a quenching circuit and two comparators. The quenching circuit is actually a set of transistors with an adjustable gate voltage. For the current work, these quenching transistors can be approximated as a resistor with a value in the 1 kΩ to 10 MΩ range, with the resistance selectable by changing the gate voltage of the transistors. The two SPAD-coupled comparators have adjustable thresholds and are connected to the start and stop signals of a short-range TDC with 48 output codes. Both the start and stop signals can be delayed on chip, which aids in both extending the TDC range and characterizing the TDC jitter (delay elements are not shown in Fig. 2). The stop signal can also be chosen from an external source, which is used for characterization of the TDC. The TDC is based on [9]. A micrograph of the complete chip can be found in Fig. 3.

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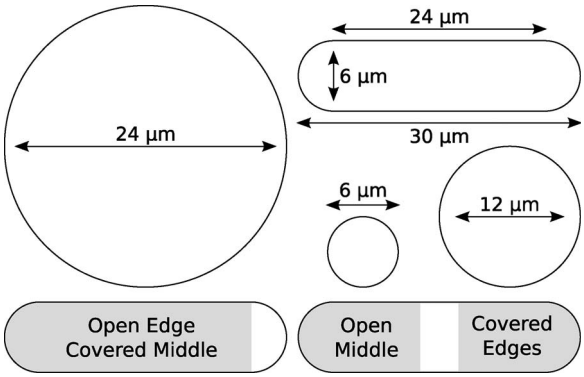

Fig. 1. SPAD geometries—three circular (middle) geometries and a pill-shaped (top right) geometry are on the test chip. The circular geometries have p+ implants with diameters of 24, 12, or 6 μm, with the guard ring outside this implant. The pill-shaped SPAD has a 6 × 24 μm rectangle capped by two semicircles, both with a diameter of 6 μm. Pill-shaped SPADs that are metal covered except for an edge (bottom left) or the middle (bottom right) are also included on the chip.

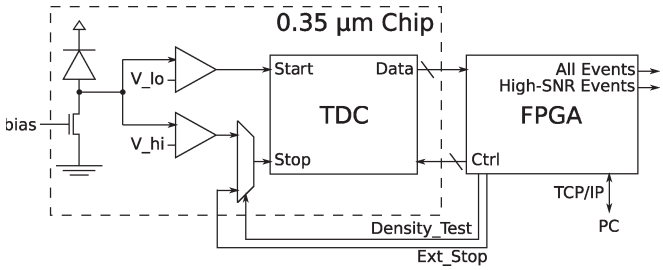

Fig. 2. Simplified system diagram—the system's major components are a test chip, an FPGA and a PC. The test chip contains pixels with an SPAD, MOSFETs acting as a variable resistance, two SPAD-coupled comparators, a TDC, and logic to allow a density test of the TDC. The FPGA contains an Ethernet link to a PC and outputs two streams of synchronous events from the SPAD: one stream contains all events and the other contains events with high SNR characteristics.

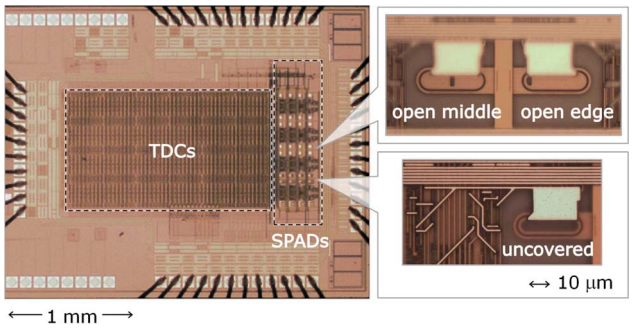

Fig. 3. Chip micrograph—a micrograph of the complete chip (left), partially covered pill-shaped SPADs (top right), and completely open pill-shaped SPAD (bottom right) is shown. The dimensions of the pill-shaped SPADs can be found in Fig. 1.

A Xilinx ML507 board is the basis for the read-out system. The board contains a field-programmable gate array (FPGA) that controls the TDC and interfaces to a PC via an Ethernet link. The FPGA can select which SPAD geometry is examined (not shown in Fig. 2). The FPGA outputs two streams of pulses synchronous with observed avalanches; one stream contains all observed avalanches, and the other stream contains a real-time, noise-reduced stream of avalanches based on a programmable lookup table. The lookup table contains whether to label an avalanche as noise based on the originating location; it is created using an offline brute-force algorithm that finds the best possible SNR at a particular light level.

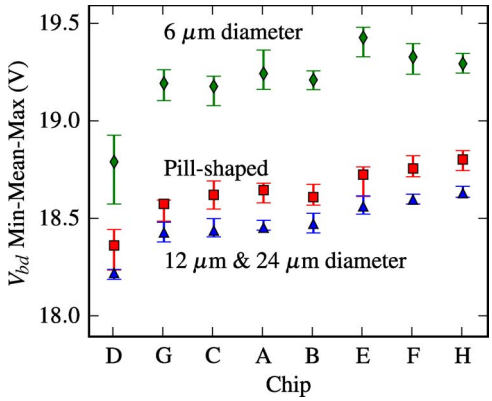

Fig. 4. Static variations in breakdown voltage are shown for eight chips. The SPADs are divided into the following groups: 6-μm-diameter diodes, with three per chip; 6 × 30 μm pill-shaped diodes, with 12 per chip; and 12- or 24-μm-diameter diodes, with three of each diameter per chip. The error bars show the minimum and maximum $V_{\rm bd}$ of a particular SPAD type on each chip, and the symbol is at the mean $V_{\rm bd}$. Measurements were performed in a dark temperature chamber at 25 °C.

III. Measuring Fabrication Nonidealities

This section contains experimentally measured values of the breakdown voltage and active area, and the section also characterizes an effect that reduces the active area.

A. Breakdown Voltage

An avalanche diode's breakdown voltage is the voltage at which an injected carrier's expected number of ionization-generated carriers exceeds one [10]. When this condition is met, the diode is in Geiger mode, and a properly quenched SPAD will create voltage and current pulses, with the pulses synchronous to the arrival of single photons.

There are several methods to measure the breakdown voltage of a SPAD *in situ*. The simplest way is to sweep the SPAD's applied voltage until a coupled comparator outputs pulses and then subtract the comparator's threshold. Fig. 4 shows breakdown voltage results for different SPADs from eight chips with this "sweep-and-subtract" method with a threshold of 100 mV. Table I contains quantitative measures of the breakdown voltage variations at 25 °C. The breakdown voltage greatly varied from geometry to geometry, with the breakdown voltages of all 24-μm-diameter diodes lower than the breakdown voltages of any 6-μm-diameter diode. The circular diodes with a diameter of either 12 or 24 μm had an average breakdown voltage of roughly 18.48 V, the average $V_{\rm bd}$ for the pill-shaped SPADs was about 18.65 V, and the small circular diodes with a diameter of 6 μm had an average breakdown voltage of 19.21 V. The chip-to-chip variation is larger than the intrachip variation for all geometries, with the chip-to-chip variation having a standard deviation between 100 and 200 mV, compared to the intrachip variation, which is lower than 100 mV. The range of breakdown voltages also varies with the geometry, with a

TABLE I
BREAKDOWN VOLTAGE CHARACTERISTICS OF DIFFERENT SPAD GEOMETRIES FROM EIGHT CHIPS IN A TEMPERATURE CHAMBER AT 25 °C ARE SUMMARIZED. EACH CHIP CONTAINS 3 SMALL CIRCULAR SPADs (6-μm DIAMETER), 6 LARGE CIRCULAR SPADs (12- OR 24-μm DIAMETER), AND 12 PILL-SHAPED SPADs (ROUGHLY 6 × 30 μm)

	SPAD Geometry		
	Large Circular	Pill-shaped	Small Circular
Mean V_{bd}	18.48 V	18.64 V	19.21 V
Maximum V_{bd}	18.69 V	18.85 V	19.50 V
Minimum V_{bd}	18.19 V	18.29 V	18.70 V
V_{bd} Range	0.50 V	0.55 V	0.81 V
V_{bd} Std. Dev.	0.12 V	0.13 V	0.19 V
Intra-chip variation (mean of chips' V_{bd} std. dev.)	**0.02 V**	**0.04 V**	**0.07 V**
Inter-chip variation (std. dev. of chips' mean V_{bd})	**0.12 V**	**0.13 V**	**0.18 V**

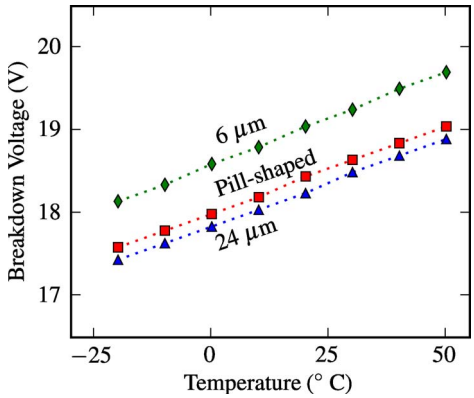

Fig. 5. Breakdown voltage variations versus temperature are shown for a small circular (top), pill-shaped (center), and large circular (bottom) SPAD from chip B. Measurements were performed in a lit temperature chamber; the level of light remained constant during the measurement, and was sufficient to cause avalanche rates above DCR between 1 and 100 kHz when the SPADs were at 25 °C and had an excess bias of 2 V.

breakdown voltage range of almost 1 V for the small circular diodes. Measurements imply that the geometry-to-geometry $V_{\rm bd}$ variations are independent of temperature, as Fig. 5 shows. The $V_{\rm bd}$ present variation is smaller than previously measured results for different structures, although the effect could simply be a temperature effect [11].

B. Inactive Distance

As described in the previous section, there is a static variation in breakdown voltage between SPADs with different geometries. The evidence implies that a static effect raises the breakdown voltage in smaller diodes. Increasing the deep n-well doping would lower the breakdown voltage, implying that the smaller diodes have a lower doping in their n-wells. However, it is unlikely that variations in the deep n-well implantation would cause the observed variations in breakdown voltage. If that were the case, then the minimum $V_{\rm bd}$ of the 6-μm-diameter diodes should roughly match the minimum $V_{\rm bd}$ of the larger circular diodes.

It has been previously proposed that the electric field distortion caused by the depletion region extending from the guard ring into the active area can cause an inactive distance and

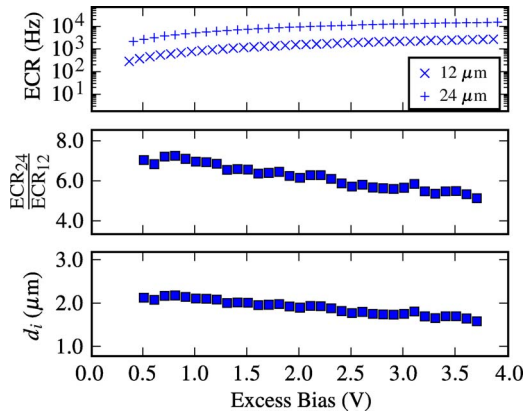

Fig. 6. Inactive distance estimate—by observing the ECR differences of a 24-μm-diameter diode and a 12-μm-diameter diode under light (top), the ECR ratio (middle) can be used to estimate the inactive distance (bottom) from the implant diffusion of the guard rings. Measurements were performed at room temperature.

distort the breakdown voltage [12]. However, as the depletion region width increases with excess bias, this effect would cause any inactive distance to increase with excess bias, contrary to the result that will be presented in Fig. 6. Additionally, the depletion region's width in the n-type silicon should be at a maximum when the p-type silicon is most highly doped; using the standard formulas and assuming an abrupt one-sided junction, this width can be estimated to be at most 800 nm [10]. Any measurement of an inactive distance larger than 800 nm would imply that the depletion region is not responsible, as Fig. 6 will also show.

The variation-causing effect appears to be stronger when more of the active area of a device is close to a guard ring, which implies that the guard ring's fabrication is involved with the effect. The circular diode that is 6 μm in diameter has the largest shift, with a smaller shift occurring for the pill-shaped SPADs that are 6 μm wide. Diffusion of the guard rings' implants could cause exactly this effect. The circular diode with a 6-μm diameter would have a larger $V_{\rm bd}$ shift than the pill-shaped SPAD, since the middle of the circular diode's active area would have a larger change in doping than the middle of the pill-shaped SPAD. The diffusion of the guard rings' implants must be negligible after a distance under 6 μm; otherwise, the 12-μm-diameter SPAD would also show a large shift in $V_{\rm bd}$ compared to the 24-μm-diameter SPAD, which is not the case. However, the ratio of photon-sensitive area between the 24- and 12-μm-diameter devices would have to be different than the expected ratio of four, as the proposed diffusion of the guard rings' implants would cause a gradual increase in breakdown voltage near the guard rings. This will be modeled as a single inactive distance d_i next to the guard rings. Further evidence that the guard rings' fabrication causes the inactive distance can be provided by checking if the dark count rate (DCR) density and photon detection probability (PDP) of SPADs with different geometries require compensation for this inactive distance to match.

Implant diffusion is proposed to compensate the n-well doping a distance d_i near the guard rings, creating a portion of the diode with a higher breakdown voltage. However, as the

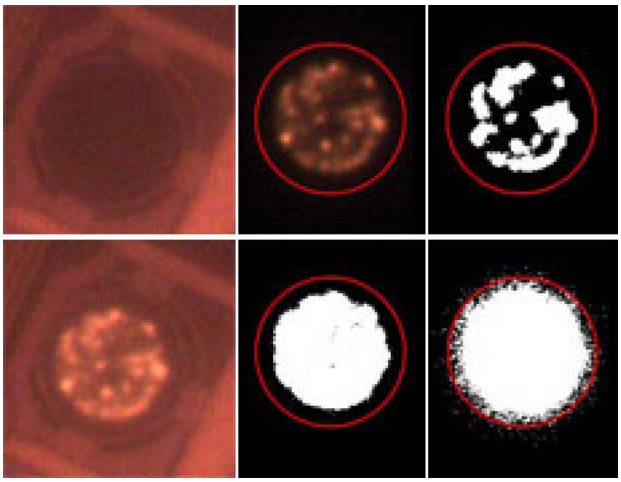

Fig. 7. Light emission from a 24-μm diode that is properly quenched (top left with chip area under external light) or improperly quenched (bottom left with chip area under external light, top middle with chip area under no light) is shown. The improperly quenched diode's light emission was thresholded at increasing values (top right, bottom middle, bottom right) to provide additional evidence for the inactive space, and also to check that premature edge breakdown was not occurring. The guard ring's location is shown with a red circle (middle, right). The diode was improperly quenched by using a quenching resistance of roughly 1 kΩ instead of roughly 1 MΩ.

CMOS process details are not available, it is not clear if the diffusion, scattering, or inaccuracy of the implants are actual causes. To provide evidence for this hypothesis, the excess count rate (ECR), which is the count rate above the DCR, can be compared for a 24-μm-diameter diode and a 12-μm-diameter diode. The inactive distance d_i and ECR ratio r follow the relation

$$r = \frac{\text{ECR}_{24}}{\text{ECR}_{12}} = \frac{\pi(12 - d_i)^2}{\pi(6 - d_i)^2} \tag{1}$$

which implies that the measured inactive distance (in micrometers) is

$$d_i = (6\sqrt{r} - 12)/(\sqrt{r} - 1). \tag{2}$$

To measure the inactive distance, a blue LED was placed 60 cm distant from a chip in a chamber with no light sources other than the LED. To ensure that the dead time, which is the time the diode takes to return to idle following an avalanche and after-pulsing, which is self-correlated noise caused by fabrication defects, did not distort the inactive distance estimate, the dead time was kept between 500 ns and 2 μs at excess biases above 1 V, and the total count rate was kept below 50 kHz. The LED was initially turned off, the breakdown voltage was measured as previously described in Section III-A, and the DCR was acquired for a 12-μm-diameter diode and a 24-μm-diameter diode. The LED was then turned on to a specific light level that remained constant. The count rate was acquired for excess biases between 200 mV and 4.0 V, and the DCR was subtracted from the measured count rate to yield the ECR (top plot of Fig. 6). The ECR ratios at various excess biases were compared to yield an estimate of the inactive distance (middle and bottom plots of Fig. 6). The light emission from an improperly quenched 24-μm diode, shown in Fig. 7, provides additional evidence of the inactive distance. Comparing the location of the guard ring with the location of the emitted light, an inactive distance that is just larger than 2 μm is obtained, which is in good agreement with the data at low excess biases in Fig. 6.

Additional evidence for the inactive distance distorting the active area will be provided in Section IV-B, when the DCR densities and PDP show a better match between the SPADs with different geometries after compensating for the inactive distance.

Estimating the inactive distance is critical to obtaining the correct active area for the PDP and noise measurements. A inactive distance of 2 μm will reduce the active area by more than 60% in the pill-shaped diode. Additional evidence for an active area distortion can be found in [13], which reports that the DCR ratio between a 4-μm-diameter diode and a 10-μm-diameter diode does not scale as expected.

It is worth noting that STI-bound SPADs are likely to be free of this effect [14]. However, some STI-bound SPADs have additional implantation layers near the STI for several purposes; these layers' effects on the active area remain to be observed [15].

IV. Characterization

This section contains the characterization data for the TDC and SPADs. The SPAD section contains a focus on matching the data between different SPAD geometries.

A. TDC

A standard density test was used to characterize the short-range TDC at a resolution of 20 ps [16]. At this resolution, the 48-code TDC's range is 0.96 ns. Dark counts from the SPAD and the clock from the FPGA were used as the start and stop signals. The event rate remained below 40 kHz during the TDC characterization. The start bias line was externally compensated for process and temperature variations. The worst-case differential nonlinearity (DNL) for this operating condition remains under 1.1 LSB. The worst-case integral nonlinearity (INL) for TDCs from three chips was 2 LSB when operating between -25 °C to 50 °C. The jitter of the TDC was found to be negligible by setting the two comparators coupled to the SPAD to trigger at the same voltage, delaying the stop signal using buffers on chip, and observing that >99.9% of events had the same code in this condition. Metastable codes occurred in less than 0.1% of events from any tested TDC.

B. Conventional SPAD Characterization

This section contains the conventional SPAD characterization, including uncorrelated noise, correlated noise, and PDP, with a focus on ensuring the inactive distance measurements are correct.

1) Uncorrelated Noise: In an SPAD in the dark, silicon traps and tunneling can cause avalanches, with the DCR being the frequency of the dark avalanches. The DCR depends on many factors, including the electric field in the diode and the number of defects present in the silicon.

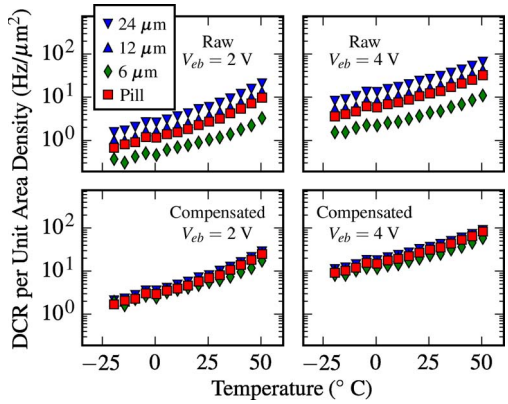

Fig. 8. DCR density versus temperature curves from four low-noise SPADs, each with a different geometry, are shown, for both raw data (top) and compensated for the inactive distance (bottom). The plots show data from SPADs at an excess bias of either 2 (left) or 4 V (right).

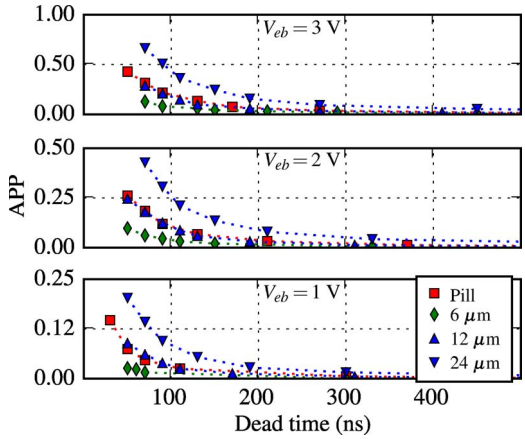

Fig. 9. After-pulsing curves are shown for different SPADs at an excess bias of 3 (top), 2 (middle), or 1 V (bottom). The SPADs with larger areas and larger currents during an avalanche tend to have larger APPs.

To measure the DCR, a chip was placed in a temperature chamber with no sources of light. The dead time was kept constant between 500 ns and 2 μs. The breakdown voltage was found, the SPAD was placed at an excess bias of 2 or 4 V, and then, the DCR was acquired for four low-noise diodes. Fig. 8 shows the raw DCR and also the following normalization for the inactive distance. The DCR density varies from just above 1 Hz/μm at -25 °C when the excess bias is 2 V to just under 100 Hz/μm at 50 °C when the excess bias is 4 V.

2) After Pulsing: To estimate the after-pulsing probability (APP), a histogram of the time between avalanches was created. Similar to previously reported results, after pulsing was found to be negligible after 500 ns [11]. An exponential fit was made to the interavalanche times greater than 1 μs, and all interavalanche times were then compared to this curve, with the fraction of the curve area above this fit yielding the APP for a specific dead time. Results are shown for all geometries and several excess biases in Fig. 9. Increasing the size of the active area, increasing the excess bias, or decreasing the dead time would be expected to increase the after pulsing.

3) PDP: To measure the PDP, light output from a monochromator (Oriel/Newport part 77250) was fed into an integration sphere (Oriel/Newport part 819D-SL-2) with a reference

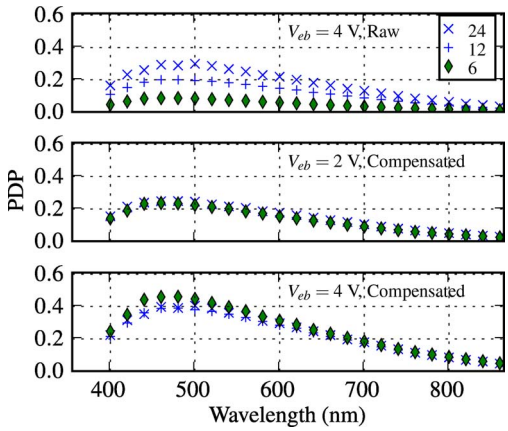

Fig. 10. Photon detection probability versus wavelength is shown for three circular SPADs (legend contains diameter in micrometers) at various excess biases. The plots are either uncompensated (top) or compensated (nontop) for the inactive distance (see Fig. 6).

diode (Hamamatsu part S1226-BQ) at one of the sphere's ports and the SPAD under test at the other. Due to the sensitivity of the diodes, a neutral density filter was placed between the SPAD and the integrating sphere. High-pass filters were placed between the integration sphere and the monochromator to ensure that light at lower harmonics from the monochromator did not interfere with the measurements. In this setup, the ripples commonly seen from the optical stack are not present, as the light is incident from many angles, not just orthogonally [17].

The SPAD's DCR was acquired with the same method listed in Section IV-B-1. The photon flux was determined by measuring the current observed by the reference diode for a specific power of incident light and then matching the photon flux predicted by the reference diode's data sheet to this current. The PDP, shown in Fig. 10, was determined by dividing the SPAD's ECR by the photon flux, compensated for attenuation caused by the neutral density filter. The SPAD's dead time was kept between 500 ns and 2 μs to ensure that after pulsing did not distort the PDP.

As would be expected from the results in Section III-B, the PDPs for the circular diodes, particularly the 6-μm-diameter diode, are quite poor when the active area is not compensated for the inactive distance. Following compensation, the results from the 12- and 24-μm-diameter diodes are in excellent agreement. The 6-μm-diameter diameter diode's PDP does not match as well; a possible explanation is that the inactive distance estimation from the 12- and 24-μm diodes does not match that of the 6-μm diode.

C. Position-Sensitive Characterization

This section contains the results from the characterization of the position-sensitive SPAD and describes the experimentally measured noise reduction.

The entire system was placed in a temperature chamber at 25 °C. The pill-shaped SPADs were placed at an excess bias of 2.5 V, which included compensation for nonuniformities in the SPAD's breakdown voltages described in Fig. 4. The low and high thresholds of the SPAD-coupled comparators were set at 0.1 and 2.0 V, respectively. The voltage rise times were acquired

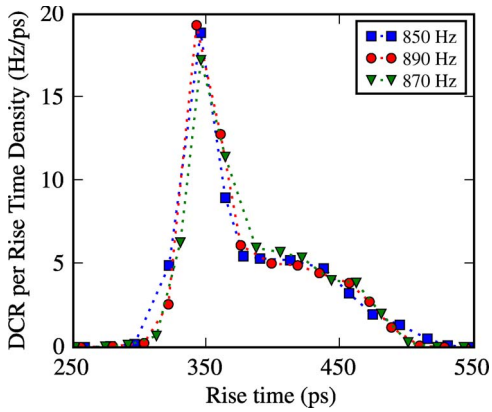

Fig. 11. DCR density histograms for SPADs are shown for three low-noise pill-shaped SPADs from chip D. The SPADs were operated at an excess bias of 2.5 V (compensated for shifts in a diode's $V_{\rm bd}$), and with the comparators at thresholds of 0.1 and 2.0 V. The entire system was in a dark temperature chamber at 25 °C. The curves have been compensated for nonuniformities in the TDCs' DNL curves, and all curves have been shifted to have the DCR density peak at a value of roughly 350 ps for easy comparison of the shapes.

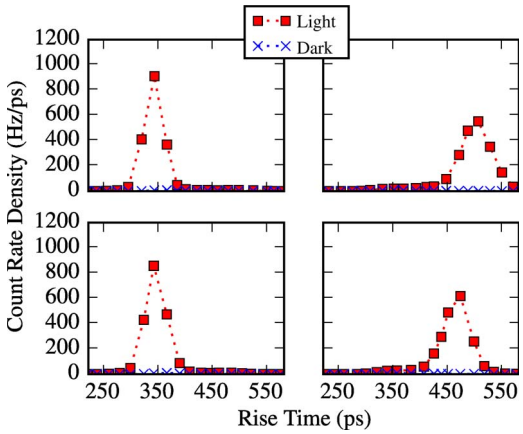

Fig. 12. Count rate histograms for differing trigger locations are shown for center-triggered (left) or edge-triggered (right) SPADs from chip H (top) or chip D (bottom). The operating conditions for the measurement system and compensations to the data are identical to the ones listed in Fig. 11, but sufficient light to cause an ECR of roughly 40 kHz was incident on the diodes in the "light" condition.

for three low-noise diodes, with Fig. 11 showing a histogram of the event rate density. The larger amount of short rise times may be caused by the slowing of the avalanche propagation as the avalanche spreads [7].

The chip-D and chip-H diodes that are covered except for the edge or the middle were then placed under light, and the histogram event rate density was acquired. Chips D and H were chosen to see if there was a large effect from the breakdown voltage variation, even though a specific excess bias was chosen. Note that the excess bias includes compensation for shifts in $V_{\rm bd}$, so the applied voltage was roughly half a volt higher to chip H than to chip D (see Fig. 4).

Fig. 12 shows the histograms of event rate density from the two chips. There is a difference of roughly 20 ps between the rise times of the edge-triggered diodes from the different chips. Additionally, the edge-triggered diodes appear to have a higher variation in rise time than the middle-triggered diodes. It is not clear if this is caused by the fact that more ionization

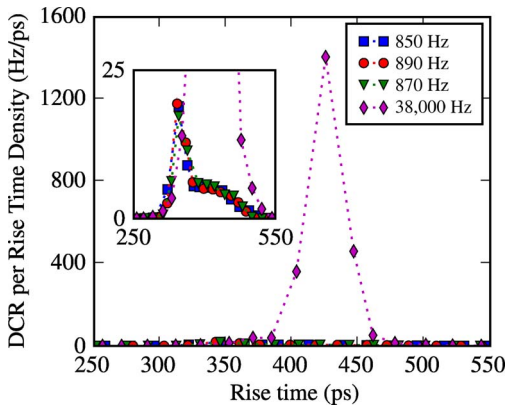

Fig. 13. High-noise SPAD's rise-time histogram is compared to the rise-time histograms of three low-noise SPADs. The inset focuses on the low-noise diodes' rise-time histograms and is identical to Fig. 11. The large spike in the high-noise SPAD's rise-time histogram corresponds to avalanches initiated closer an edge of the diode's major axis than the middle. The operating conditions for the measurement system and compensations to the data are identical to those listed in Fig. 11.

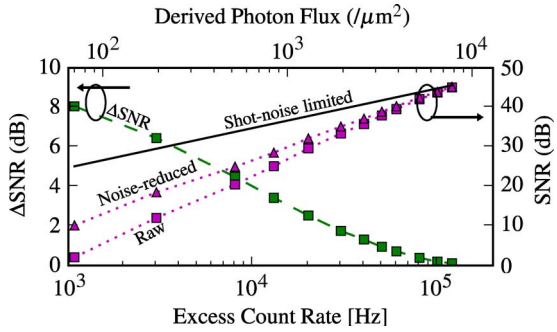

Fig. 14. SNR increase versus incident light is shown for a diode with a noise rate of 38 kHz. Operating conditions are identical to those in Fig. 12, except that a variable amount of blue light (abscissa) was incident on the SPAD. Photon fluxes were derived with an assumed PDP of 30% (see Fig. 10). A higher SNR (right ordinate) is better.

occurs or if there is a larger variation in position caused by the coverings. Additionally, there may also be an effect due to the edge's exposure to more of the guard ring, which would raise the breakdown voltage at the major edge of the pill-shaped SPAD. Studies with STI-bound SPADs are likely to aid in discriminating between the effects.

Fig. 13 shows the histogram of DCR density for three low-noise diodes and one high-noise diode. As expected, the histogram from the high-noise diode contains a large spike. It seems that a fixed-position defect is causing most of the noise in this diode. Operating this diode with longer dead times did not have a sizable effect on the noise; it appears that the after-pulsing-causing mechanism is different than the mechanism causing most of this diode's noise.

With the SNR defined as

$$\mathrm{SNR} = 20\log_{10}\left(\frac{\mu_{\rm sig}}{\sigma_{\rm sig}}\right) \tag{3}$$

where $\mu_{\rm sig}$ is the mean, and $\sigma_{\rm sig}$ is the standard deviation of the avalanche count during an integration time of 1 s, Fig. 14 shows the experimentally measured SNR with and without the noise reduction (described in Section II), along with the change

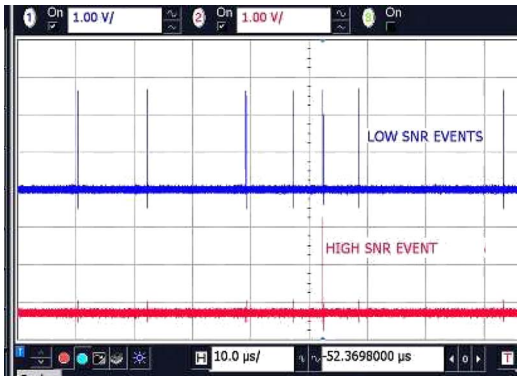

Fig. 15. Oscilloscope trace of noise reduction is shown as output by a real-time processing block on the FPGA.

TABLE II
CHARACTERIZATION SUMMARY OF 24 PILL-SHAPED SPADs AND 12 PVT-COMPENSATED TDCs

	Property	Value
SPAD	Mean Breakdown Voltage	18.6 V
	Breakdown Voltage Std. Dev.	0.17 V
	Median Dark Count	840 Hz
	After-pulsing	$<$ 1 %
TDC	resolution	20 ps
	TDC area	100 x 1,450 μm^2
	$\lvert$mean DNL$\rvert$	$<$0.01 LSB
	DNL std. dev.	0.3 LSB
	worst $\lvert$DNL$\rvert$	$<$1.1 LSB
	worst $\lvert$INL$\rvert$	$<$2.0 LSB
	jitter	negligible
Chip	Area	2 x 2.5 mm^2
	Power	60 mW
	Best, Measured SNR Gain	8 dB

in SNR. The change in SNR varies from roughly $+8$ dB at low light levels to $+0$ dB at high photon fluxes. At higher light levels, the shot-noise from the signal dominates the variance, and hence, the noise becomes less critical to the SNR. The lookup table and processing functionality can be added to the FPGA, allowing the creation of a noise-reduced synchronous pulse stream. Fig. 15 displays an oscilloscope trace of a stream with all avalanches and a noise-reduced stream, as output by a real-time processing component on the FPGA.

A summary of the characterization data can be found in Table II.

Unfortunately, due to the position sensitivity relying on the ionization-noise-distorted avalanche spread, the uncertainty in position is quite high. Thus, a large fraction of the active area must be sacrificed to reduce the noise, giving poorer performance than might be expected in photon-starved environments. Additionally, the position sensitivity across the diode appears to lack uniformity, with greater sensitivity near the edges of the diodes. The noise-reduced diode, which had a defect near the edge, is likely to be a better candidate for noise reduction than diodes with defects in the middle. No SPADs with defects in the middle were observed across the eight chips, and thus, experimental results cannot be compared.

This particular technique might be useful for applications requiring single-photon capability, high timing resolution, and the capability to operate in environments with high numbers of fixed-position defects, such as rangefinding in space. However, there are a number of open-ended issues pertaining to whether the realized chip could meet the proposed application, including how resistant the other components are to radiation, how temperature dependent the technique is, and how effective the technique would be in relation to a non-noise-reduced SPAD.

V. CONCLUSION

Experimental data for position-sensitive SPADs integrated in a standard 0.35-μm CMOS process have been presented. For the standard characterization, the PDP is seen to peak at almost 40% for an excess bias of 4 V and wavelengths just shorter than 500 nm, with a roughly linear decrease to PDPs less than 5% for wavelengths of roughly 900 nm. Other standard results, such as the APP and DCR, have been presented, with results being as expected for the different geometries.

The rise time of the voltage observed by the quenching circuitry is seen to be between 130 and 150 ps. A fixed-position defect appears to be causing most of the noise in a high-noise diode. An SNR increase of 8 dB for the same diode under low light levels has been measured, with the capability to process this information in real time on an FPGA and output a noise-reduced pulse stream.

Given all the drawbacks of position-sensitive devices and the poor performance of the noise reduction technique, it seems unlikely that this method will be more useful than simply switching off the noisy diodes. Attempts to use position sensitivity in the circular diodes have proven to be problematic and were not included in the present publication. Previous work with the devices used quenching circuitry that was more complex than passive quenching, and extending the position-sensitive technique based on voltage rise times to larger devices would probably require more complex quenching circuitry [3].

Despite these drawbacks, the technique may be useful for studying the types of noise inherent in diodes. For example, previous evidence overwhelmingly implies that lattice defects cause after pulsing; the portion of the present technique used in isolating noise from signal may also be useful for measuring whether the majority of after-pulsing is caused by a few fixed-position defects or whether the sources of after pulsing are spread out over the entire area of the diode [18]. An integrated solution may also prove useful for studying avalanche propagation and noise sources at cryogenic temperatures. Even though position-sensitive avalanche diodes' use in the mainstream is unlikely, the devices show promise for studying a number of phenomenon associated with the diodes themselves.

REFERENCES

[1] L. Carrara, C. Niclass, N. Scheidegger, H. Shea, and E. Charbon, "A gamma, X-ray and high energy proton radiation-tolerant CIS for space applications," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 40–41.

[2] I. Rech, I. Labanca, G. Armellini, A. Gulinatti, M. Ghioni, and S. Cova, "Operation of silicon single photon avalanche diodes at cryogenic temperature," *Rev. Sci. Instrum.*, vol. 78, no. 6, p. 063 105, Jun. 2007.

[3] G. Ripamonti, S. Cova, M. Ghioni, M. Mastrapasqua, and S. Vanoli, "(PS) ^{2}: A new semiconductor device for positron-sensitive picosecond detection of single optical photons," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 310, no. 1/2, pp. 184–188, Dec. 1991.

[4] D. R. Schaart, S. Seifert, R. Vinke, H. T. van Dam, P. Dendooven, H. Lhner, and F. J. Beekman, "LaBr3: Ce and SiPMs for time-of-flight PET: Achieving 100 ps coincidence resolving time," *Phys. Med. Biol.*, vol. 55, no. 7, pp. N179–N189, Apr. 2010.

[5] D. Stoppa, D. Mosconi, L. Pancheri, and L. Gonzo, "Single-photon avalanche diode CMOS sensor for time-resolved fluorescence measurements," *IEEE Sensors J.*, vol. 9, no. 9, pp. 1084–1090, Sep. 2009.

[6] B. Rae, C. Griffin, K. Muir, J. Girkin, E. Gu, D. Renshaw, E. Charbon, M. Dawson, and R. Henderson, "A microsystem for time-resolved fluorescence analysis using CMOS single-photon avalanche diodes and microleds," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 166–603.

[7] A. Spinelli and A. Lacaita, "Physics and numerical simulation of single photon avalanche diodes," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1931–1943, Nov. 1997.

[8] J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach, and R. Henderson, "A 32 $\times$ 32 50 ps resolution 10 bit time to digital converter array in 130 nm CMOS for time correlated imaging," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 77–80.

[9] P. Dudek, S. Szczepanski, and J. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, Feb. 2000.

[10] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley-Interscience, 1981.

[11] A. Gulinatti, I. Rech, P. Maccagnani, M. Ghioni, and S. Cova, "Large-area avalanche diodes for picosecond time-correlated photon counting," in *Proc. 35th Eur. Solid-State Device Res. Conf.*, Sep. 2005, pp. 355–358.

[12] N. Faramarzpour, M. Deen, S. Shirani, and Q. Fang, "Fully integrated single photon avalanche diode detector in standard CMOS 0.18-μm technology," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 760–767, Mar. 2008.

[13] C. Niclass, M. Sergio, and E. Charbon, "A single photon avalanche diode array fabricated in 0.35-μm CMOS and based on an event-driven readout for TCSPC experiments," in *Proc. SPIE*, W. Becker, Ed., 2006, vol. 6372, no. 1, p. 637 20S.

[14] H. Finkelstein, M. Hsu, and S. Esener, "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology," *IEEE Electron Device Lett.*, vol. 27, no. 11, pp. 887–889, Nov. 2006.

[15] M. Gersbach, J. Richardson, E. Mazaleyrat, S. Hardillier, C. Niclass, R. Henderson, L. Grant, and E. Charbon, "A low-noise single-photon detector implemented in a 130 nm CMOS imaging process," *Solid State Electron.*, vol. 53, no. 7, pp. 803–808, Jul. 2009.

[16] B. Swann, B. Blalock, L. Clonts, D. Binkley, J. Rochelle, E. Breeding, and K. Baldwin, "A 100-ps time-resolution CMOS time-to-digital converter for positron emission tomography imaging applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1839–1852, Nov. 2004.

[17] R. Wolffenbuttel, "Integrated silicon colour sensors," Ph.D. dissertation, Delft Univ. Technol., Delft, The Netherlands, 1988.

[18] A. Rochas, "Single photon avalanche diodes in CMOS technology," Ph.D. dissertation, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2003.

Matthew W. Fishburn, photograph and biography not available at the time of publication.

Yuki Maruyama, photograph and biography not available at the time of publication.

Edoardo Charbon, photograph and biography not available at the time of publication.