A Single Photon Detector Implemented in a 130nm CMOS Imaging Process

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***Abstract*— We report on a new single photon avalanche diode (SPAD) fabricated in a 130nm CMOS imaging process. A novel circular structure combining shallow trench isolation (STI) and a passivation implant creates an effective guard ring against premature edge breakdown. Thanks to this guard ring, unprecedented levels of miniaturization may be reached at no cost of added noise, decreased sensitivity or timing resolution. The detector integrated along with quenching and read out electronics was fully characterized. Optical measurements show the effectiveness of the guard ring and the high degree of electric field planarity across the sensitive region of the detector. With a photon detection probability of up to 30% and a timing jitter of 125 ps at full-width-half-maximum this SPAD is well suited for applications such as 3-D imaging, fluorescence lifetime imaging and biophotonics.**

I. INTRODUCTION

Since the first implementations of single photon avalanche diodes [1] and CMOS-based SPADs [2], these devices have established themselves amongst the detectors of choice in multiple time-correlated imaging methods such as fluorescence lifetime imaging and 3D imaging. One of the major challenges still remaining is the creation of large arrays of SPADs. This implies the reduction of pitch and the full scalability of detectors. In addition, to reach picosecond time resolutions it is generally necessary to perform time discrimination off chip. With thousands or millions of single photon detectors, the bottleneck becomes readout, unless timing electronics is integrated on chip [3]. To allow for sufficient electronics to be integrated on pixel or array level, the solution is either designing SPADs in deep-submicron CMOS technology or using 3D packaging technology.

II. SPAD IMPLEMENTATION

In this paper we present a novel SPAD structure implemented in a dedicated 130nm imaging CMOS process [4]. The core of the SPAD consists of a p-n junction biased above its breakdown voltage, thus operating in Geiger mode. In this regime of operation, free carriers, such as photogenerated electron-hole pairs, can trigger an avalanche breakdown by impact ionization. To avoid premature edge breakdown a guard ring has been implemented limiting the electric field at the edges of the junction. Due to its geometry, the use of STI as a guard ring yields a significant improvement in fill-factor [5]. It is however well-known that STI dramatically increases the density of deep-level carrier generation centers at its interface. Thus, if the active region of the SPAD is in direct contact with the STI as in [5], the injection of free carriers into the sensitive region of the detector results in a very high count rate, known as dark count rate (DCR), unrelated to photo-detection events.

In this paper we propose a technique to reduce DCR in STI-bound SPADs, while maintaining the high-density promise of STI-based implementations. In our approach, the STI region is surrounded by several passivation implants, creating a glove-like p-type structure that surrounds the STI. At the STI interface the doping level is high, resulting in a very short mean free path of the minority carriers. This has the effect of drastically reducing the probability of these carriers entering the active region of the SPAD. With increasing distance from the STI, the p-type doping concentration is reduced in order to minimize the electric field between the guard ring and the n-well, thus reducing the probability of edge breakdown.

Because of design constraints, only octagonal SPADs have been designed in deep-submicron technologies so far [5][6]. At the edges of such octagonal structures the electric field is significantly higher than in the rest of the multiplication region, thus creating regions of high noise contribution. To ensure a uniform electric field distribution across the entire p-n junction, a circular geometry was implemented for the SPAD presented here. The availability of a buried n-type implant allows for an ohmic contact to the n-well to be made. A schematic representation of the SPAD can be seen in Fig. 1 and a photomicrograph of the detector with integrated electronics is shown in Fig.2.

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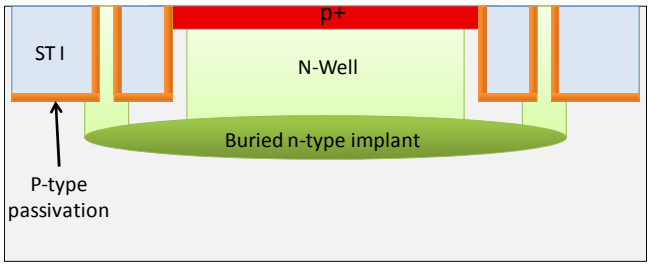

Figure 1. Cross-Section of the circular STI-bound SPAD (not to scale). The STI-interface is passivated using mutliple p-type implants, thus reducing the probability of minority carriers entering the multiplication region and triggering dark counts.

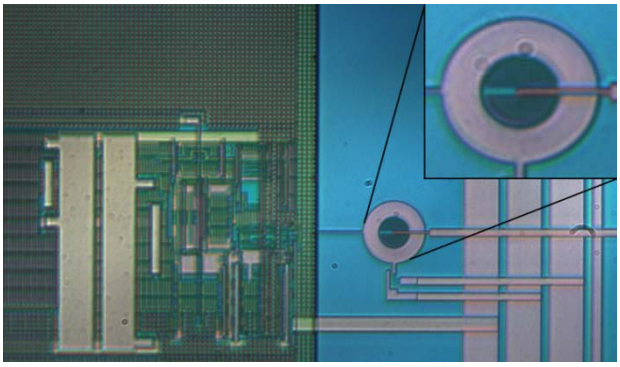

Figure 2. Photomicrogarph of the SPAD and the integrated test electronics implemented in 130nm CMOS technology.

The SPAD presented here has been integrated along with an on-chip ballast resistor and a comparator. The ballast resistance R_Q in Fig. 3 is used to perform passive quenching and recharge of the diode when operating in Geiger mode. Voltage VOP satisfies the equation

$$VOP = V_e + |-V_{BD}|,$$

where V_e is the excess bias voltage and V_{BD} is the breakdown voltage. When an avalanche breakdown is triggered, the avalanche current flowing through the ballast resistance decreases the voltage across the diode. When this voltage reaches the breakdown voltage, the avalanche current is no longer sustained and is quenched. The SPAD is then passively recharged by a small current flowing through the ballast resistance. The comparator, with proper threshold voltage V_{th}, is used to convert the Geiger pulses into digital signals.

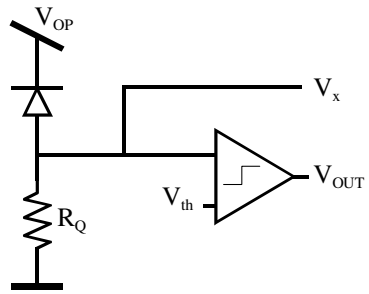

Figure 3. Schematic Diagram of the SPAD and testing electronics. The passive quenching circuit was designed as a ballast resistor. Recharge is achieved passively through the same component. Threshold detection and impedance conversion is implemented via a fast comparator.

III. CHARACTERIZATION

For a p-n junction to work well in Geiger mode it must exhibit a low dark current and an abrupt breakdown behavior. The I-V characteristic was measured statically using a standard semiconductor analyzer. Fig. 4 shows that the dark current is $5x10^{-11}$A at the breakdown voltage of 9.4V.

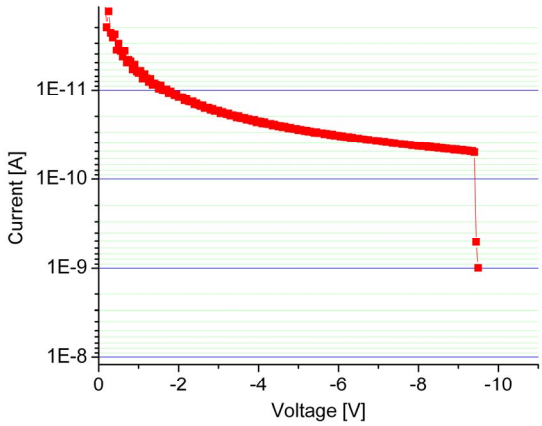

Figure 4. I-V Characteristic of the SPAD.

Even though a more advanced CMOS process was used, the novel guard ring structure and the implementation of round SPADs allowed for a drastic reduction of DCR from approximately 1 MHz in [5] to about 90 kHz at room temperature and 1 volt of excess bias, whilst increasing the active area of the SPAD. While the DCR is similar to the device in [6], the STI-based guard ring structure allows for a significant improvement in fill-factor as shown in [5]. When compared to older technologies, the use of advanced CMOS technologies implies higher doping levels as well as reduced annealing and drive-in diffusion steps. These factors contribute heavily to the noise floor measured in deep-submicron SPADs. Fig. 5 shows the temperature dependence of the DCR, the slope indicates that due to the high doping levels, tunneling-induced dark counts are the dominating noise source over trap-assisted thermal generation. Fig. 6 shows the dark count rate at room temperature as a function of the excess bias voltage.

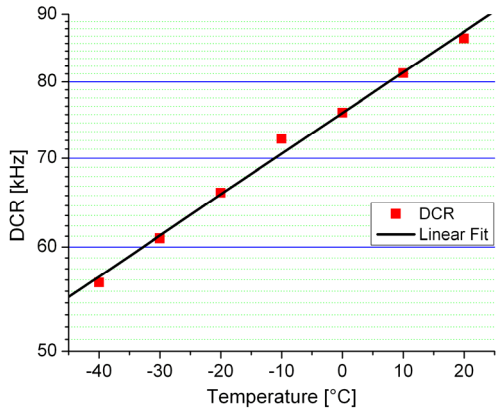

Figure 5. Dark count rate of the SPAD in function of temperature at 1V of excess bias voltage. The slope of the curve indicates that tunneling is the dominant noise source.

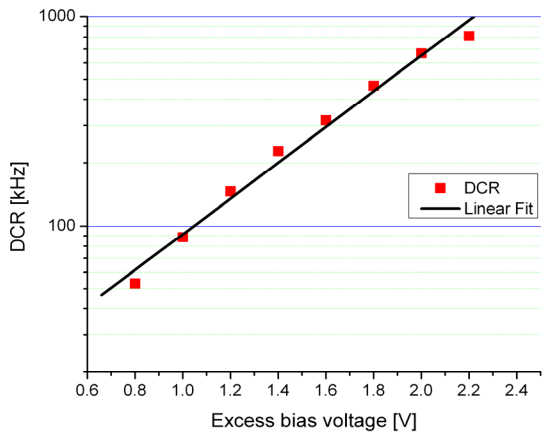

Figure 6. Dark Count Rate at room temperature as a function of the excess bias voltage.

To prove the effectiveness of the guard ring and the homogeneity of the electric field across the active region of our device, an optical measurement of the photons emitted during avalanche breakdown was undertaken. The emission of photons during avalanche breakdown is directly proportional to the current intensity and thus to the electric field. During a period of 16s a continuous avalanche current, limited to 100 µA, was allowed to flow through the diode and photoemission was captured using a microscope and a standard CCD camera.

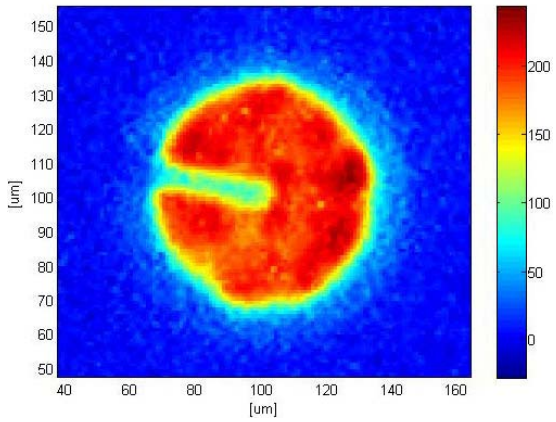

Figure 7. Measurement of the photoemission intensity (arbitrary scale) across the SPAD during avalanche breakdown. Uniform emission indiates equal probability of breakdown on the active area.

The photoemission shown in Fig. 7 indicates that the electrical field is distributed homogeneously across the sensitive region of the SPAD. Furthermore, the absence of significant emission peaks at the border of the active region shows that the guard ring is effective in lowering the electric field at the borders of the detector. Note that the region with low emission intensity going to the center of the detector was shielded by a metal line connecting the center of the p+ implant.

The sensitivity of the SPAD over a wide spectral range has also been investigated. The use of an imaging CMOS process gives access to an optimized optical stack and thus allows for a good photon detection probability (PDP). The measured PDP peaks at 30% at 480nm of wavelength for an excess bias voltage of 2V. As a comparison, the SPAD fabricated in standard 0.18µm technology in [7] achieved a maximum PDP of only 5.5% at 2V of excess bias. The measurements were obtained using a standard monochromator system coupled to an integrating sphere (LOT Oriel Group Europa) and a calibration detector (Hamatsu).

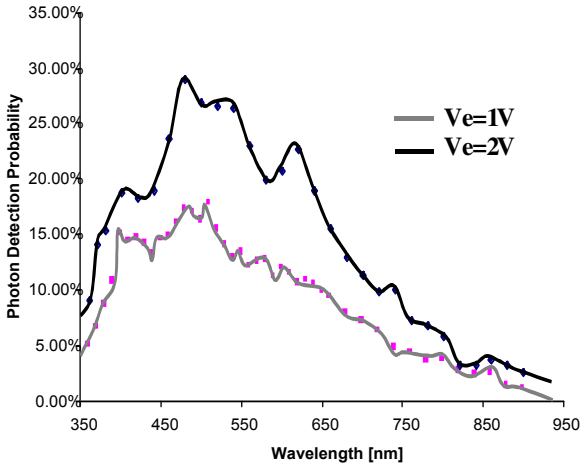

Figure 8. Photon detection probability for two different excess bias voltages.

Another important measure for time-correlated applications is the time response of the detector. To assess its time-resolution, the SPAD was illuminated by a picosecond laser diode source with 637nm of wavelength (Advanced Laser Diode Systems GmBH, Berlin, Germany). At 1V of excess bias voltage, the timing jitter of the entire system at full-width-half-maximum was measured to be 125ps. As can be seen from the right-hand side of the measured time response in Fig. 9, the absorption of photons underneath the active region of the SPAD creates a tail in the time response as the generated free carriers may diffuse back into the multiplication region.

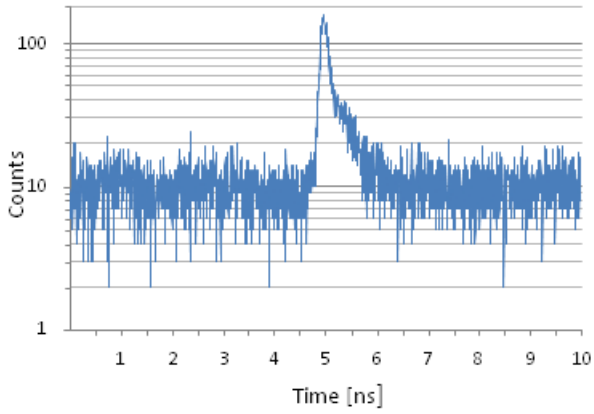

Figure 9. Time response of the SPAD when illuminated by a picosesond light source at 637nm wavelength and 1V of excess bias voltage.

During an avalanche breakdown event, a significant amount of charge carriers flow through the diode. Some of these carriers may be trapped in the multiplication region of the diode and subsequently released, thus triggering a second avalanche breakdown. To limit the probability of such afterpulses, it is necessary to limit the amount of charges flowing through the diode during an avalanche breakdown event; this can be done by limiting the capacitance at the borders of the diode. In our case, the use of a CMOS process allows the on-chip integration of the quenching resistance and of the read-out electronics at the immediate surroundings of the detector, thus limiting the parasitic capacitances.

To assess the afterpulsing probability the correlation between subsequent breakdown events was measured. Fig. 10 shows the autocorrelation curve obtained. Note that after each breakdown event the SPAD needs to recharge and is thus inactive for a certain amount time, known as dead time. For the structure presented here the dead time is ~180ns. Therefore, in the first 180ns after a breakdown event, the autocorrelation is zero. When the SPAD is fully recharged the autocorrelation is stable around one, proving that no afterpulsing is present.

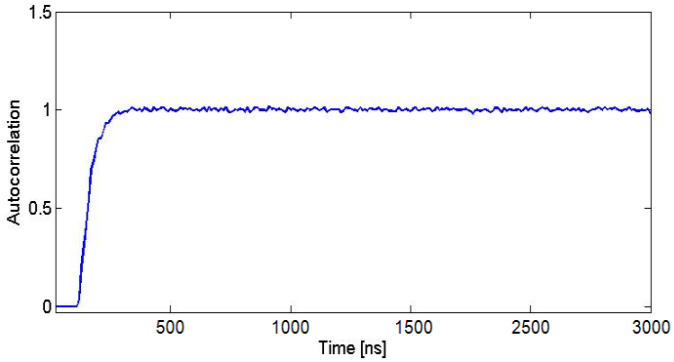

Figure 10. Autocorrelation probability of the SPAD. No afterpulsing contribution could be measured.

The performance of the detector presented in this paper is summarized in Table 1.

TABLE I. PERFORMANCE SUMMARY AT ROOM TEMPERATURE

Performance	Min.	Typ.	Max.	Unit
PDP @ Ve = 1V			18	%
PDP @ Ve = 2V			30	%
DCR @ Ve = 1V		90		kHz
DCR @ Ve = 2V		670		kHz
Active area		58		μm^2
FWHM Time jitter @ Ve = 1V		125		ps
Afterpulsing probability		<1		%
Dead time		180		ns
Breakdown voltage		9.4		V

IV. CONCLUSION

The SPAD presented in this paper combines the advantages of deep-submicron processes, such as the possibility of integrating complex electronics and the improved fill-factor thank to a STI-based guard ring, while improving the noise performance of more than an order of magnitude when compared to comparable STI-bound SPADs. The first integration of SPADs along with quenching and read-out electronics in 130nm CMOS technology presented here allowed showing the absence of afterpulsing for a detector dead time of 180ns. Finally, optical measurements of the photoemission during avalanche breakdown proved the effectiveness of the guard ring structure and the planarity of the multiplication region.

DISCLAIMER

This publication reflects only the authors' views. The European Community is not liable for any use that may be made of the information contained herein.

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