

Single-Photon Synchronous Detection

Cristiano Niclass, Claudio Favi, Theo Kluter, Frédéric Monnier, and Edoardo Charbon

Ecole Polytechnique Fédérale de Lausanne
CH-1015 Lausanne
SWITZERLAND

Abstract¹—A novel imaging technique is proposed for fully digital detection of phase and intensity of light. A fully integrated camera implementing the new technique was fabricated in a 0.35 μm CMOS technology. When coupled to a modulated light source, the camera can be used to accurately and rapidly reconstruct a 3D scene by evaluating the time-of-flight of the light reflected by a target. In passive mode, it allows building differential phase maps of reflection patterns for image enhancement purposes. Tests show the suitability of the technique and confirm phase accuracy predictions.

I. INTRODUCTION

Evaluation of intensity and phase of an impinging ray of multi- or monochromatic light has shown its usefulness in a number of applications. One of the first applications of phase-based imaging has been historically optical rangefinding, where the time-of-flight (TOF) of a reflected ray of light is computed from the phase difference between an outgoing and an incoming optical signal. Traditionally, the evaluation of the phase of a light source is performed using techniques similar to homodyne and heterodyne receivers in radio frequency systems. In these devices the incoming radio signal is replaced with the impinging optical signal and the local oscillator with an electrical or optical signal synchronized with the outgoing modulated light source. The two signals are mixed and low-pass filtered, generally *in situ*, to obtain an intermediate frequency or baseband signal proportional to the phase difference between outgoing and incoming light.

Both CCD and CMOS implementations of this technique exist and have been commercially available for some time now [1],[2],[3],[4]. In these devices pixel-level mixing is performed during a light modulation cycle by selectively redirecting photocharges that are partially in and out of phase onto different locations for accumulation. In this approach, carrier selection and accumulation is limited by the relatively slow diffusion process below the photogate, thus limiting the time resolution of the measurement in each modulation cycle. In addition, due to the small number of charges in play in each cycle, generally millions of cycles are necessary to achieve reasonable phase accuracy. Consequently, the accumulation process may last tens of milliseconds to tens of seconds before TOF can be determined.

Several techniques have been proposed to increase the time resolution up to a few nanoseconds in CCDs [5] and in

CMOS [6]. However, all these methods still suffer from the fact that the phase signal is analog and thus it needs amplification and A/D conversion on a pixel-by-pixel basis. As a result, several sources of noise and non-idealities are present and may be severe. Moreover, in this approach background illumination can in principle be eliminated by virtue of the fact that it appears as a common-mode signal across the differential signal of each detector. However, when saturation is reached, the differential signal begins to compress, causing background effects to resurface and contrast to be slashed.

In this paper we propose a fully digital, multi-pixel phase detection method based on single-photon avalanche diodes (SPADs). We call this method single-photon synchronous detection (SPSD). In this method, a photon detected by a SPAD triggers a digital pulse that is accumulated in a digital counter. The charge redirection of conventional methods is replaced with a simple demultiplexer. Different locations for accumulation are replaced with as many independent counters. The phase can thus be computed by a simple manipulation of the counter outputs at the end of the accumulation period.

There are several advantages of SPSPD if compared to conventional modulation based phase detection methods. First, the time resolution of a partial phase measurement during a modulation cycle is far superior, since it is dominated by the time resolution of a SPAD, typically a few tens of picosecond [7]. Thus, in principle a much smaller number of cycles are sufficient to achieve the same overall phase accuracy. Second, due to the digital nature of the phase measurement, no errors are introduced during the accumulation period, except for unavoidable Poisson noise. Moreover, the lack of amplification and A/D conversions removes quantization errors and the usual non-idealities associated with these components. Third, saturation is inherently prevented by detecting overflow in the counter and thus stopping accumulation on a pixel basis. This method, unlike global saturation control techniques (such as e.g. [3]), is both simple and accurate, and can be performed entirely digitally. Finally, the device is amenable to implementing multiple access techniques to enable coexisting rangefinding systems in close proximity based, for example, on FDMA or CDMA [9].

A camera implementing the proposed SPSPD technique was fabricated in a 0.35 μm CMOS technology. The camera comprises an array of 60x48 85x85 μm^2 fully scalable pixels. Unlike recent implementations of SPAD arrays operating based on the TCSPC technique [8], the SPSPD camera takes

¹ This work was supported by a grant in the framework of the Innovation Network initiative from EPFL (Innogrants).

advantage of full pixel parallelism. Thus in principle, no photons impinging upon the detector area are lost, if separated by at least the dead time of a SPAD. The camera was tested on a TOF rangefinder setup yielding a resolution of approximately 3.3cm with a frame rate of 22fps. The light source was achieved by sinusoidal modulation of an array of LEDs operating at 30MHz with a mean optical power of 800mW.

II. SINGLE-PHOTON SYNCHRONOUS DETECTION

The SPSD technique, introduced in [9] and described in detail in [10], involves the demodulation of the phase shift an optical signal experiences when travelling from source to target and back to the sensor. Figure 1 shows the basic setup involved in a solid-state 3D imager based on SPSD. It consists of a periodically modulated light source, typically a sine wave, used to illuminate the objects in front of the 3D image sensor, imaging optics, a band-pass filter used to block background light, and a single-photon image sensor comprising pixel-wise demodulation circuitry.

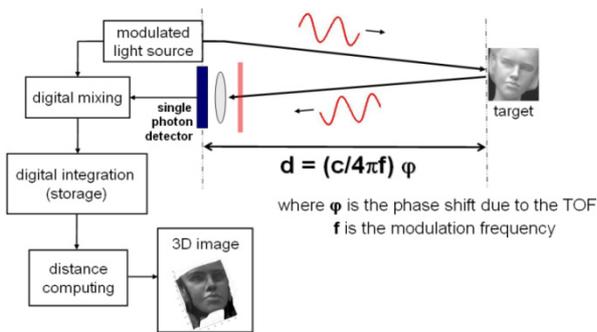


Figure 1. Solid-state 3D imaging setup based on the SPSD technique.

Thanks to the digital nature of single-photon detectors, phase demodulation may be achieved digitally. It involves a digital mixing operation with a reference signal, shared by the illumination source, and integration over a high number of cycles. Conveniently, these operations are implemented in a SPSD sensor by means of a demultiplexer (or a switch), driven synchronously with the reference signal, that connects the single-photon detector to two or more counters. When a photon is detected, depending on its arrival time with respect to the reference signal period, it increments a given counter. As a high number photons are detected, the contents of the counters follow a distribution that reproduces the optical signal waveform, over one reference period. Based on these values, it is possible to determine the phase, amplitude and offset of the optical signal.

In order to unambiguously demodulate the signal phase, at least, three counters are theoretically necessary. Practically, it is possible however to use only two counters and generate four samples. Figure 2 shows an example of illumination and demodulation waveforms, as adopted in this work. The sensor operates in an interlaced detection scheme based on two acquisition phases. In the first acquisition phase, the pixel-level demultiplexer switches between two counters so as to generate two samples, C_0 and C_{180} , corresponding to 0° and 180° of phase with respect S_{MOD} . Once these two samples are acquired and readout, the sensor operates in the second acquisition phase, in which S_{MOD} is delayed by a quarter of period with respect to the reference signal. As a result, the same in-pixel counters are used to acquire samples C_{90} and C_{270} , corresponding to 90°

and 270° of phase. Note that, although only two counters are used, the demodulation circuit does not miss any photon detection, unless the counter maximum value is reached.

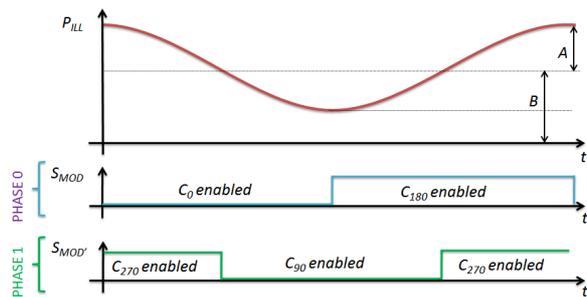


Figure 2. Incident optical signal and demodulation waveforms.

Once the four samples are acquired, the amplitude A , offset B , and phase φ are determined as

$$A = \frac{\sqrt{(C_{270} - C_{90})^2 + (C_0 - C_{180})^2}}{2}, \quad (1)$$

$$B = \frac{C_0 + C_{90} + C_{180} + C_{270}}{4}, \quad (2)$$

$$\varphi = \arctan\left(\frac{C_{270} - C_{90}}{C_0 - C_{180}}\right). \quad (3)$$

Although φ is the most important result for a TOF rangefinder, A and B also carry interesting pixel information. A may be conveniently used to determine whether a pixel signal, in a given acquisition frame, has a sufficiently strong amplitude so as to be considered as a reliable measurement. Indeed, pixel signals with negligible amplitude could be simply disregarded. B may also be used to compute intensity images.

Theoretically, in Equations (1)-(3), all the four samples $\{C_i\}$ are assumed to be acquired simultaneously. When the objects in the scene are not static, the acquisition of four samples based on two counters may suffer from augmented motion artifacts. In order to solve this problem, the acquisition of C_0/C_{180} and of C_{90}/C_{270} should be interlaced at frequency sufficiently high that moving objects appear static and thus affects all $\{C_i\}$ simultaneously. Note that conventional motion artifacts may persist depending on the actual frame rate achieved by the image sensor.

III. IMAGE SENSOR ARCHITECTURE

The image sensor proposed in this work takes advantage of a fully digital realization, from photon detection to depth imaging. A simplified block diagram of the image sensor is shown in Figure 3. It consists of an array of 60×48 single-photon pixels, each one comprising its own SPSD demodulation circuit based on two 8-bit counters. The sensor also includes a bias generation circuit, a JTAG controller for testing/characterization purposes, and a readout circuit. The readout circuit is based on a controller that allows the image sensor to operate autonomously, only requiring a clock signal. The pixel matrix area is divided in 8 blocks, each one consisting of 8×48 pixels and being handled by an independent readout block. The first and last readout blocks handle six active and two blocked columns each. A decoder, driven by the readout controller, selects a row. In that row, a pipelined sequence of readout and reset is achieved in the 8 blocks in parallel, thanks to the 8 digital output buses of 16 bits implemented. In each row, the

readout sequence is operated as follows. The first pixels in all the 8 blocks are read out, then, when the second pixels in all the blocks are read out, the first ones are simultaneously reset to zero. When the readout circuit finishes reading out the eighth pixels in all the blocks, it spends one additional cycle to reset them, before switching to the next row. As a result, 9 cycles of clock are necessary to read out and reset a full row. Since the sensor comprises 48 rows, the full frame rolling readout requires exactly 432 cycles. Note that in each readout cycle a digital signal, $IDX[8:0]$, indicates the address of the pixels in the blocks that are currently being read out, and that each 16-bit bus outputs the contents of the two in-pixel counters simultaneously.

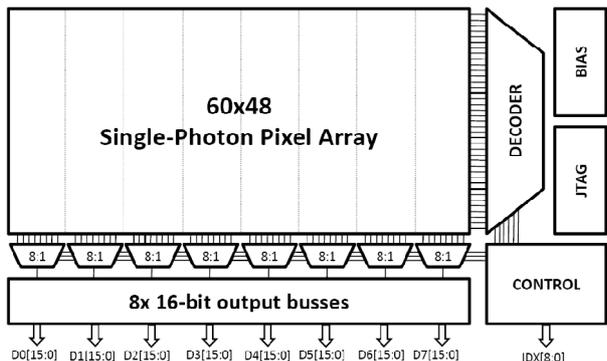


Figure 3. Block diagram of the image sensor. The sensor consists of a 60x48 pixel array, a JTAG controller, and a fast parallel readout circuitry.

The readout circuit was designed to run at a clock frequency of up to 40MHz. At that frequency, a frame acquisition and readout takes 10.8 μ s. This time is short enough to be used in the interlaced acquisition of C_0/C_{180} and C_{90}/C_{270} , thus preventing motion artifacts as described previously. Moreover, since a pixel may be read out and reset in only 10.8 μ s, its 8-bit counters hardly ever reach their maximum values, assuming a dead time of 40ns.

IV. SINGLE-PHOTON PIXEL

A. Front-end Circuit

Single-photon detection with high timing resolution is achieved by means of a SPAD detector, whose performance characterization was reported in [11]. This device was carefully designed for the 0.35 μ m CMOS technology used in this work. Its front-end circuit involves 8 MOS transistors that perform passive quenching and active recharge. Figure 4 shows the schematics of the complete pixel circuit. Active quenching is achieved by adequately choosing two different thresholds for the inverter and nor gates [10]. At the inverter output, a digital inverted pulse reflects the detection of a photon. Its leading edge, i.e. high-to-low transition, accurately indicates the arrival time of the photon.

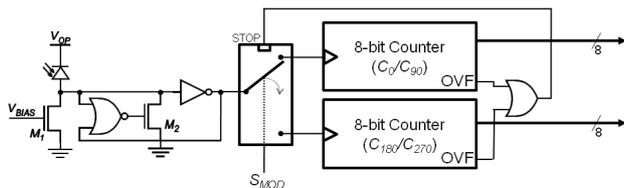


Figure 4. Pixel circuit comprising front-end and digital demodulation. Passive quenching and active recharge ensures higher dynamic range with little impact on pixel size. Fully digital implementation enables noise-free demodulation and readout.

B. Demodulation Circuit

As shown in Figure 4, the demodulation circuit consists of a 2:1 demultiplexer driven by a global signal S_{MOD} , synchronized with the light source, and two 8-bit counters. Each counter has a parallel tri-state output bus and a signal, OVF, indicating that the next increment would result in an overflow state. The OVF signals of both counters are combined, via an OR gate, to block the demultiplexer in a state in which neither counters could be incremented. Once one counter reaches its maximum value, the pixel is blocked until the next readout and reset operation.

V. EXPERIMENTAL RESULTS

The fabricated image sensor, shown in Figure 5, has a surface of 6.5x5.5 mm².



Figure 5. Photomicrograph of the SPSP image sensor. The circuit, fabricated in 0.35 μ m CMOS technology, has a surface of 6.5x5.5mm². The pixel pitch is 85 μ m.

As can be seen in the picture, the pixel matrix area occupies most of the integrated circuit area. Global distribution of S_{MOD} is implemented symmetrically, from a pad in the center of the top part of the padding. The image sensor was then mounted on a custom prototype of a camera, based on a FPGA for data interface and USB controller to provide a link with any PC, shown in Figure 6. An additional board comprising 48 NIR LEDs emitting at 850nm wavelength was mounted on the front face of the prototype. The LEDs provided a 30MHz sine wave illumination with an average optical power of 800mW and with a field-of-view of 50°.



Figure 6. 3D camera prototype based on SPSP.

The single-photon sensor was first characterized in terms of its main source of noise, i.e. dark count rate. Figure 7 shows the distribution of DCR over all the pixels in the array. As can be seen, most of pixels exhibit a DCR of a few hundred Hertz, thus leading to a typical temporal noise contribution of a few tens of Hertz. The median value was 245Hz while the average DCR showed to be higher, at 1261Hz, due to a small number of defected pixels, similarly

to [8]. In our scheme these pixels may be ignored with no interference to surrounding pixels.

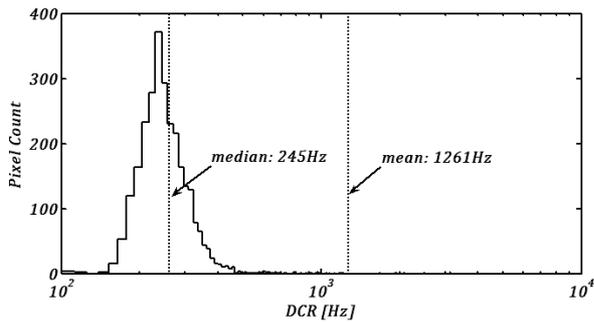


Figure 7. Distribution of DCR over 60x48 pixels under nominal V_E of 3.3V and at room temperature.

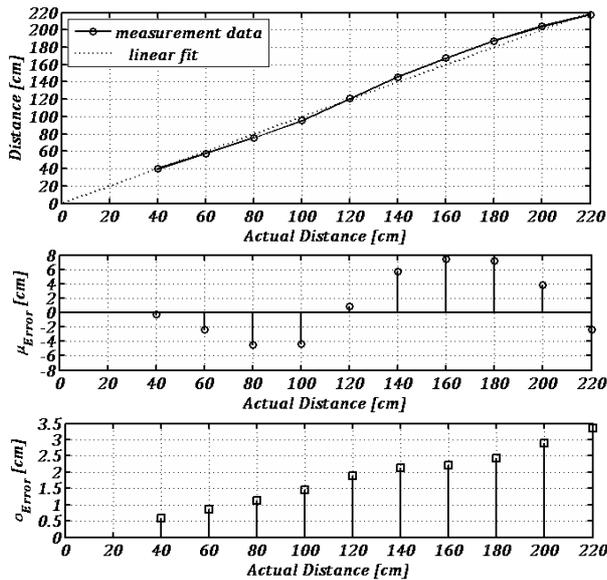


Figure 8. Measured distance versus actual distance, non-linearity (INL) and repeatability errors (1σ). Measurements based on an integration time of 45ms, i.e. 22fps.

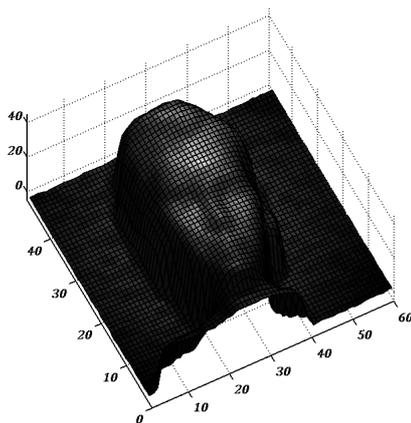


Figure 9. Experimental 3D image of a human-sized mannequin acquired with an integration time of 500ms.

The prototype was also evaluated with respect to its ranging capability. A flat panel was used as a target and displaced over a range of about 2.2m, starting at a distance of 40cm, so as to determine measurement linearity. Figure 8 shows the experimental results compared to the actual target distance. In the picture, integral non-linearity (INL) and 1σ

repeatability errors were also plotted as a function of distance. Relatively high INL was obtained due to third harmonic distortion in the illumination waveform, which resulted in aliasing effects through the SPSP demodulation based on four samples per period [10].

A 3D image of a human-sized mannequin was captured with the setup, using an integration time of 500ms. The model was placed at a distance of 1m from the prototype. A summary of performance parameters and operating conditions is given in Table I.

TABLE I. SUMMARY OF PERFORMANCE PARAMETERS

Name	Value	[Unit]
Image resolution	60x48	-
Median DCR	245	Hz
Pixel dead-time	40	ns
Imaging lens f-number	1.4	-
Illumination central wavelength	850	nm
Narrowband optical filter width	40	nm
Illumination frequency	30	MHz
Illumination field-of-view	50	°
Illumination average power	800	mW
Resolvable distance range	5	m
Integration time	45	ms
Maximum distance INL up to 2.2m	7.4	cm
Maximum 1σ distance resolution at 2.2m	3.3	cm
Maximum ASIC feasible framerate ^{a,b}	46296	fps

a. assuming a complete SPSP demodulation per frame
b. currently not achieved due to prototype limitations

REFERENCES

- [1] R. Miyagawa and T. Kanade, "CCD-Based Range-Finding Sensor", *IEEE Trans. on Electron Devices*, Vol. 44, N. 10, pp. 1648-1652, Oct. 1997.
- [2] R. Lange, "3D Time-of-Flight Distance Measurement with Custom Solid-State Image Sensors in CMOS/CCD-Technology", Ph.D. Dissertation, ETH-Zürich, Switzerland, 2000.
- [3] S. Kawahto, I. A. Halin, T. Ushinaga, T. Sawada, M. Homma, Y. Maeda, "A CMOS Time-of-flight Range Image Sensor with Gates-on-field-oxide Structure", *IEEE Sensors Journal*, 2007.
- [4] B. Buxbaum, R. Schwarte, T. Ringbeck, M. Grothof, and X. Luan, "MSM-PMD as Correlation Receiver in a New 3D-Imaging System", in U. Schreiber, C. Wener, G. W. Kamerman, and U. N. Singh, Eds., *Proc. SPIE*, Vol. 4546, pp. 145-153, Jan. 2002.
- [5] R. Büttgen, "Extending Time-of-Flight Optical 3D-Imaging to Extreme Operating Conditions", Ph.D. Dissertation, Univ. of Neuchatel, Switzerland, 2007.
- [6] C. Bamji and E. Charbon, "Methods for CMOS-Compatible Three Dimensional Image Sensing using Quantum Efficiency Modulation", U.S. Patent 6,515,740, Feb. 2003.
- [7] C. Niclass and E. Charbon, "A CMOS Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging", *Intl. Solid-State Circuit Conference (ISSCC)*, pp. 364-365, Feb. 2005.
- [8] C. Niclass, C. Favi, T. Kluter, M. Gersbach, E. Charbon, "A 128x128 Single-Photon Imager with on-Chip Column-Level 97ps 10bit Time-to-Digital Converter Array", *Intl. Solid-State Circuit Conference (ISSCC)*, pp. 44-45, Feb. 2008.
- [9] C. Niclass, "Method and arrangement for measuring the distance to an object", U.S. Patent Application 182,949, 2007.
- [10] C. Niclass, "Single-Photon Image Sensors in CMOS: Picosecond Resolution for 3D Imaging", Ph.D. Dissertation No. 4161, EPFL, Switzerland, 2008.
- [11] C. Niclass, M. Sergio, E. Charbon, "A single-photon avalanche diode array fabricated in 0.35 μ m CMOS and based on an event-driven readout for TCSPC experiments", APCT Conference, SPIE Optics East, Oct. 2006.