A 11 µW 0ºC-160ºC Temperature Sensor in 90 nm CMOS for Adaptive Thermal Monitoring of VLSI Circuits

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***Abstract*—This paper reports design, efficiency and measurement results of the temperature sensor based on substrate bipolar transistors and a PTAT multiplier for adaptive thermal monitoring of deep-submicron VLSI circuits. The prototype temperature sensor with un-calibrated 3σ accuracy of 0.9ºC within a 0ºC-160ºC temperature range has been fabricated in standard single poly, six metal 90nm CMOS, consumes only 11µW at 1V power supply and measures 0.05mm^2.**

I. INTRODUCTION

The magnitude of thermal gradients and associated thermo-mechanical stress increase further as VLSI designs move into nanometer processes and multi-GHz frequencies [1]. Higher temperature increases the risk of damaging the devices and interconnects since major back-end and front-end reliability issues including electro-migration, time-dependent dielectric breakdown, and negative-bias temperature instability have strong dependence on temperature. Additionally, low power techniques such as dynamic power management, clock gating, voltage islands, dual V_{DD}/V_T and power gating may cause significant on-chip thermal gradients and local hot spots due to different clock/power gating activities and varying voltage scaling. Furthermore, in 3D IC designs heat and thermal problems are exacerbated as the vertically stacked multiple layers of active devices cause a rapid increase of power density. The complexity of the interconnection structures, back end of line structures and through-silicon vias increase the complexity of the conductive heat transfer paths in a stacked die structure. The thermal conductivity of the dielectric layers inserted between device layers for insulation is very low compared to silicon and metal [2] leading to temperature gradient in the vertical direction of a 3D chip. In the case of hot spots, these thermal effects are even more pronounced.

As a consequence, continuous thermal monitoring is necessary to reduce thermal damage and increase reliability. Built-in temperature sensors predict excessive junction temperatures as well as the average temperature of a die within design specifications. In order to maximize the coverage, the thermal sensing devices are scattered across the entire chip to meet the high-level die temperature control requirements. This trend of multiple monitoring circuits is evident in recent processors such as the POWER5, CELL, Itanium, and Opteron processors [3]-[6]. The sensors are networked by an underlying infrastructure, which provides the bias currents to the sensing devices, collects measurements, and performs analog to digital signal conversion. Therefore, the supporting infrastructure is an on-chip element at a global scale, growing in complexity with each emerging processor design. It needs to span a large distance covering the entire processor core, networking an increasing number of devices.

The temperature sensors for thermal monitoring of VLSI circuits should meet several requirements including compatibility with the target process with no additional fabrication steps, high accuracy, a small silicon area and low power consumption to reduce the error caused by self-heating. Temperature sensor based on time-to-digital-converter [7] is constrained by the large area and power overhead at the required sampling rate. Temperature sensor operating in the sub-threshold region [8] is prone to dynamic variations as thermal sensitivity increases by an order of magnitude when operating in sub-threshold [9]. Consequently, the majority of CMOS temperature sensors are based on the temperature characteristics of parasitic bipolar transistors [10]. In this paper, we present compact, low area, low power temperature sensor with high accuracy and wide temperature range in standard 90 nm CMOS technology based on substrate bipolar transistors and a proportional-to-absolute temperature (PTAT) multiplier.

II. CIRCUIT DESCRIPTION

To convert temperature to a digital value, a well-defined temperature-dependent signal and a temperature-independent reference signal are required. These quantities can be derived utilizing exponential characteristics of bipolar devices for both negative- and positive temperature coefficient [11]. For constant collector current, base-emitter voltage V_{be} of the bipolar transistors has negative temperature dependence around room temperature. This negative temperature dependence is cancelled by a proportional-to-absolute temperature dependence of the amplified difference of two base-emitter junctions.

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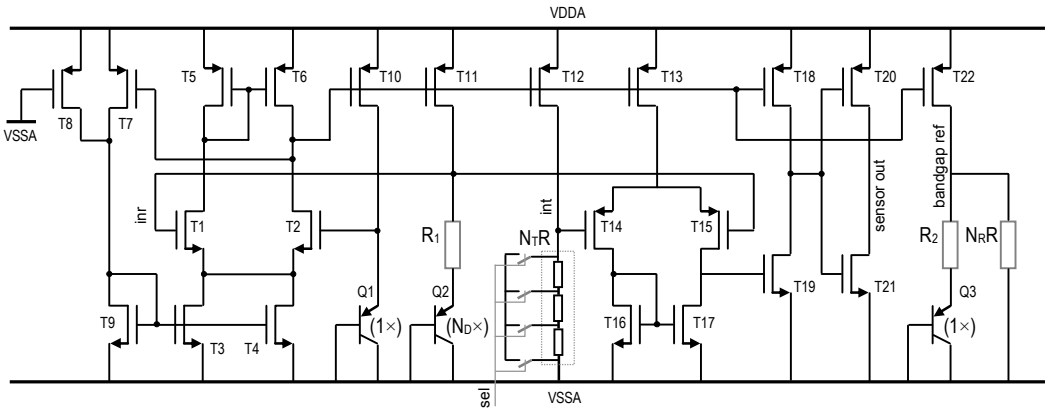

Figure 1: Temperature sensor – schematic view

These junctions are biased at fixed but at unequal current densities resulting in the relation directly proportional to the absolute temperature. This proportionality is, however, rather small (0.1-0.25mV/°C) and needs to be amplified to allow further signal processing.

A. Non-idealities of bipolar transistors

In CMOS process, both lateral and vertical (substrate) *pnp* transistors can be used as temperature sensing devices. The lateral transistors, however, have low current gains and their exponential current voltage characteristic is limited to a narrow range of currents [10]. The substrate transistors have reasonable current gains and high output resistance, but their main limitation is the series base resistance, which can be high due to the large lateral dimensions between the base contact and the effective emitter region. To minimize errors due to this base resistance, we limited the maximum collector currents through the transistors to μA level. The slope of the base-emitter voltage V_{be} of the bipolar transistors depends on process parameters and the absolute value of the collector current. To obtain an overall accuracy of ±1°C a maximum spread of V_{be} is limited to 900μV level and the maximum random voltage error in ΔV_{be} to 60μV. This spread is PTAT in nature and can be mitigated by trimming, albeit at the expense of increased manufacturing costs. In this way, a single-point trim is enough to compensate for process spread. Since intra-batch spread is usually significantly less than inter-batch spread, batch calibration offers a cheaper alternative to individual trimming, at the expense of lower accuracy.

B. Circuit implementation

The proposed temperature sensor is illustrated in Figure 1. The right part of this circuit, comprising a voltage comparator, (transistors $T_{13\text{-}21}$) creates the output signal of the temperature sensor. The rest of this circuit consists of the temperature sensing-circuit, amplifier, and start-up. The input of the comparator consists of a differential source-coupled stage, followed by two amplifying stages and one digital inverter. To enable a certain temperature detection, voltage comparator require two signals with different temperature dependence; an increasing PTAT voltage V_{int} across the resistor network N_TR (Figure 2) and decreasing PTAT voltage V_{inr} at the comparator positive input generates temperature decisions (Figure 3).

The resistors are formed by $p+$ poly resistances, which have minimum process variation and temperature coefficient in the given foundry's CMOS process.

The (nominally) zero temperature coefficient is exploited for a temperature-independent bangap-reference generation. In a bandgap voltage reference (Figure 4), an amplified version of ΔV_{be} is added to V_{be} to yield a temperature-independent reference voltage V_{ref}. The negative voltage-temperature gradient of the base-emitter junction of the transistor Q_1 is compensated by a PTAT voltage across the resistor R_1, thereby creating an almost constant reference voltage V_{ref}. The bandgap reference voltage is obtained at the output of the amplifier (rather than at its input). The PTAT voltage is firstly converted into current through transistor T_{22} and then summed up to lower reference voltage through resistor R_2. However, the curvature of V_{be} (of transistors $Q_{1\text{-}2}$) will also be present in the bandgap reference voltage [11]. For a current, which is independent of temperature, the curvature correction is in the same order of magnitude of mismatch. The first-order temperature compensation of bandgap reference voltage involves the cancellation of the temperature term by using the PTAT voltage. The second-order temperature compensation is curvature-compensated by adjusting the proportional-to-absolute temperature-type spread on V_{be} of a transistor Q_3 with adjustable resistors N_RR. In essence, based on the ratio of the resistors N_RR and R_2, the V_{be} of a junction with a constant current is subtracted with the V_{be} of a junction with the PTAT current. To accurately define this ratio, adjustable resistors N_RR are constructed of identical unit resistors.

The amplifier ($T_{1\text{-}6}$) consists of a non-cascoded OTA with positive feedback to increase the loop-gain. The amplifier output voltage is relatively independent of the supply voltage as its open-loop gain is sufficiently high. Due to the asymmetries, the inaccuracy of the circuit is mainly determined by the offset and flicker noise of the amplifier, which directly adds to ΔV_{be}. Several dynamic compensation techniques such as auto-zeroing, chopping or dynamic element matching [13] might be employed to decrease offset and flicker noise. However, inherently, such techniques require very fast amplifier, whose noise is typically several order of magnitude larger and consumes considerably more power.

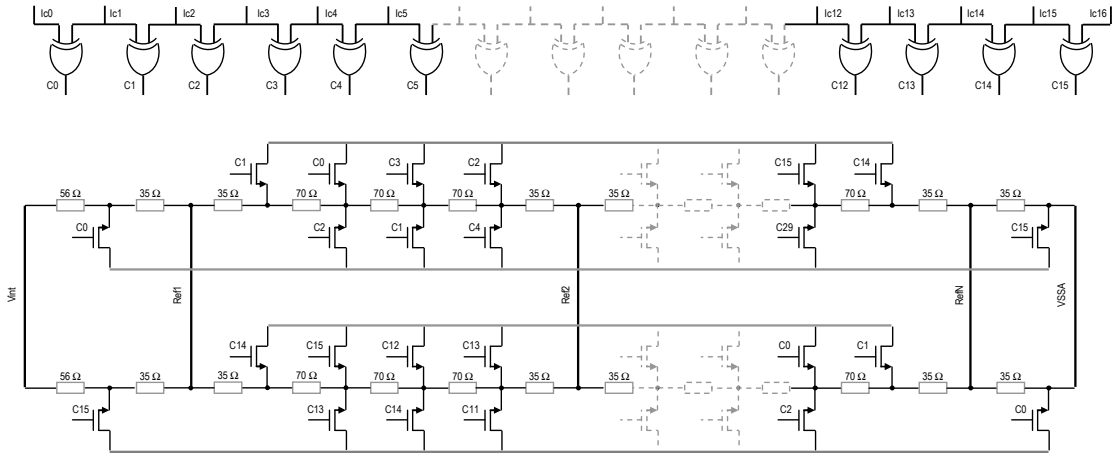

Figure 2: N_TR Resistive network – schematic view

Furthermore, chopping increases circuit complexity and adds switching noise due to e.g. charge dump and clock interference. Such characteristics make these techniques unsuitable for thermal monitoring of VLSI circuits. In this design, to lower the effect of offset to meet ±1°C accuracy, the systematic offset is minimized by adjusting transistor dimensions and bias current in the ratio, while the random offset is reduced by a symmetrical and compact layout. Additionally, the collector currents of bipolar transistors Q_1 and Q_2 are rationed by a pre-defined factor, e.g. transistors are multiple parallel connections of unit devices. The amplifier has sufficient gain to equalize its input voltages. Since these nodes are the same, the currents from these nodes to ground must be the same as well. The current through R_1 is therefore PTAT (this current is also flowing through the output transistor T_{22}).

A start-up circuit consisting of transistors $T_{7\text{-}9}$ drives the circuit out of the degenerate bias point when the supply is tuned on. The diode-connected device T_9 provides a current path from the supply through T_7 to ground upon start-up.

C. N_TR Resistive network

The scan chain delivers a four-bit thermometer code for the selection of the resistor value N_TR. As illustrated in Figure 2, the nodes in between each resistor have different voltages depending on their proximity to V_{int}. By using thermometer decoding on the digital signal one specific node can be selected as the correct analog voltage. The number of resistor elements determines the resolution of the resistor-network; an n-bit network requires a ladder with 2^n resistors. The resistor-ladder network is inherently monotonic as long as the switching elements are designed correctly. Similarly, since no high-speed operation is required, parasitic capacitors at a tap point will not create significant voltage glitch. A limit on resistor-value is set by mismatches of individual resistors, which determine the overall accuracy of the generated reference voltages. Assuming that the resistor values are normally distributed with mean R and standard deviation σ_R, the maximum mismatch σ_R/R allowed for four-bit resolution is ≤ 17.6 percent [14].

III. Experimental Results

A prototype temperature sensor with N_TR resistive network was fabricated in a standard single poly, six metal 90 nm CMOS (Figure 5). The stand-alone sensor occupies an area of 0.05 mm^2 operates within 1.0V-1.8V range and dissipates 11 µW. In the test silicon, four bits for a sixteen selection levels are chosen for the temperature settings, resulting in a temperature range from 0°C-160°C in steps of 9°C, which is sufficient for thermal monitoring of VLSI circuits (Figure 3).

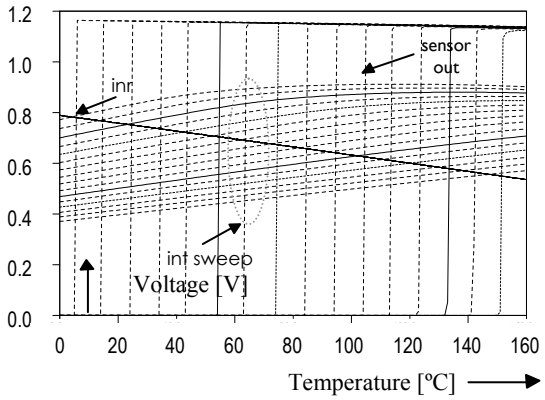

Figure 3: Sixteen selection levels in the temperature sensor

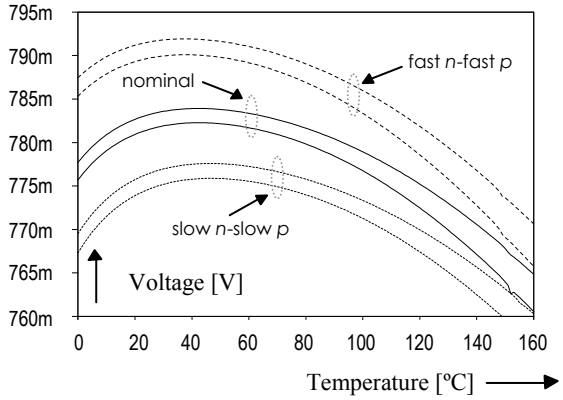

Figure 4: Bandgap reference voltage; nominal, fast-fast and slow-slow process corners

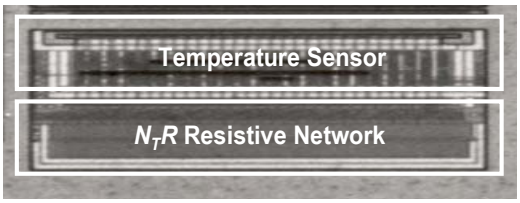

Figure 5: Chip micrograph

If more steps are required, a selection N_TR can be easily extended with higher resolution resistive network. For the robustness, the circuit is completely balanced and matched both in the layout and in the bias conditions of devices, cancelling all disturbances and non-idealities to the first order. A summary of the sensor performance and comparison with recently published works is shown in Table I. Measurements have been performed on 45 samples from 2 different batches. All chips are functional in a temperature range between 0°C and 160°C. The average error at room temperature is around 0.5°C, with a standard deviation of less than 0.4°C, which matches the expected error of 0.4°C within a batch. Non-linearity is approximately 0.4°C from 0°C to 160°C. The intrinsic base-emitter voltage non-linearity in the bandgap reference is limited by compensation circuit. The measured noise level is lower than 0.05°C.

IV. CONCLUSIONS

In this paper, the feasibility of a high accuracy, adaptive temperature sensor has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal 90 nm CMOS. The stand alone sensor intended for thermal monitoring of VLSI circuits can be easily integrated in to modern system-on-chip designs with minimal efforts, occupies a small silicon area of 0.05 mm^2, operates at 1.0V-1.8V supply voltage in a temperature range from 0°C-160°C and dissipates only 11 µW.

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	[7]	*[8]*	*[15]*	*[16]*	*[17]*	*[18]*	***[This work]***
CMOS Technology	*0.35 µm*	*1.0 µm*	*0.7 µm*	*0.18 µm*	*0.13 µm*	*65 nm*	*90 nm*
Range (ºC)	*0~100*	*10~100*	*-55~125*	*temp switch*	*0~100*	*0~100*	*0~160*
Supply voltage (V)	*3.0~3.8*	*5*	*2.5~5.5*	*1.0~1.8*	*1.2*	*1.0*	*1.0~1.8*
Inaccuracy (ºC)	*-0.7~+0.9*	*± 1*	*±0.1*	*±1.1*	*-1.8~+2.3*	*±10.0*	*± 0.9*
Sensor type	*temp-to-pulse*	*analog current*	*ΔV_{be}*	*ΔV_{be}*	*duall-DLL*	*temp-to-pulse*	*ΔV_{be}*
Calibration	*-*	*-*	*one-point*	*-*	*one-point*	*autocalibration*	*-*
Power (µW)	*10*	*300*	*247*	*13*	*12000*	*55*	*11*
Area (mm^2)	*0.175*	*0.023*	*0.16*	*0.03*	*0.16*	*0.01*	*0.05*

TABLE I– SUMMARY OF THE TEMPERATURE SENSOR PERFORMANCE AND COMPARISION WITH PRIOR ART