DIGITAL CARTESIAN FEEDBACK LINEARIZATION OF SWITCHED MODE POWER AMPLIFIERS

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ABSTRACT

The efficient use of the power budget in small satellite applications is of primary importance because of the reduced size of the power sources. Unfortunately, high efficiency in power amplifiers (PA) is strongly related to non-linearities and hence distortion. In this paper a digital architecture for the linearization of switched mode PAs is implemented, and a circuit to detect the phase shift and the CORDIC algorithm to correct that phase as well as to compute the magnitude are developed. The results show that linearity is improved by 20 dB for a system with a bandwidth of 9.6 kHz for a loop gain of 10 and 400 ns of system delay. The circuit, implemented in a FPGA consumes a total of 33.3 mW.

Index Terms— Cartesian feedback, linearization, phase alignment, CORDIC.

1. INTRODUCTION

One of the key aspects of the transmitter is a highly efficient, power agile, switching power amplifier. As a consequence of having a high efficient PA no power losses occur due to dissipation, improving the lifetime of the batteries and/or making a better use of the power delivered by the solar panels. However, the high efficiency of the switching PA has one important drawback in non-linearity. Therefore, to achieve a highly efficient switching PA in a transmitter, a mechanism to linearize it is required. A powerful means to linearize a system is the Cartesian feedback linearization technique [1]-[2], which proves to be an efficient solution to the linearization problem, although difficulties such as stability and phase shift have to be considered. The system has to be stable in order to accomplish its function, and the phase shift, introduced by delays in the system and distortion of the PA, has to be detected and corrected. Most of the previous work on Cartesian feedback have focused on linear-mode, relatively inefficient PAs such as Class A, B, AB. As a result, to improve efficiency a different class of PA such as switched mode PA is utilized.

In this paper a digital implementation of Cartesian feedback for the switched mode PA is proposed. This is a digital circuit that takes the input and feedback signals, computes the phase difference between them and generate the output signals with the adequate phase correction as well as magnitude by means of the CORDIC algorithm.

2. MIXED-SIGNAL CARTESIAN FEEDBACK

The mixed-signal Cartesian feedback system (Figure 1) consists of the digital to analog (DAC), the analog to digital (ADC) converter and the digital block for signal processing (in grey color). The low pass filter in the forward path (anti-imaging filter) is used to smooth the sampled and held signal delivered by the DAC, and the low pass filter in the feedback path (anti-aliasing filter) is used to eliminate second order harmonics of the carrier frequency that arise as a result of the down-conversion. The up and down converters modulates the quadrature signals around the carrier frequency. The supply voltage of a Class E switched mode PA is modulated using the envelope elimination restoration (EER) technique [3]. The digital block is implemented with a phase detection that computes the instant phase difference and drives an integrator which accumulates the phase shift. The rotation block performs the phase correction on the error signals. A magnitude block computes the magnitude of the error signal that drives the EER. The error signals are obtained by an addition between input signals and feedback signals.

The Cartesian feedback faces two challenges: stability and phase shift. The anti-imaging filter in the forward loop

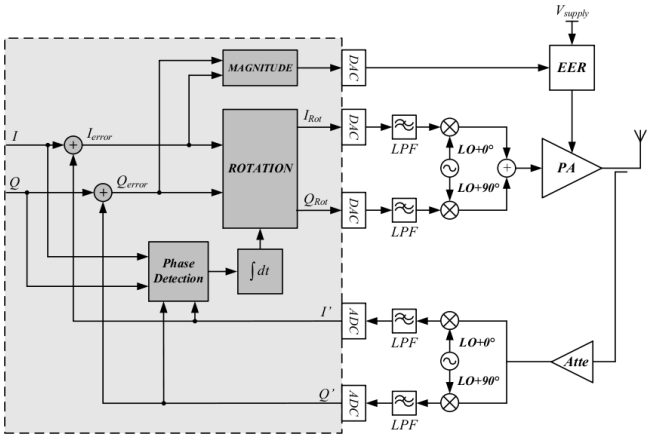


Fig. 1. Mixed-signal Cartesian feedback system.

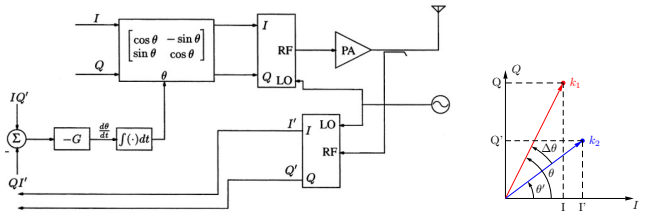


Fig. 2. Automatic phase alignment concept [4].

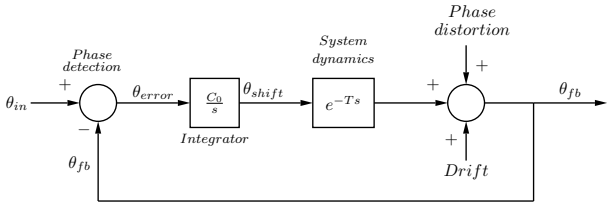


Fig. 3. Phase regulation diagram in the frequency domain.

adds two dominant poles to the system as a requirement to reduce the sampling frequency. As a consequence the system is unstable and hence compensation has to be applied. A lead compensator is included in the feedback path. The analysis by means of the root locus method is applied to locate the poles and zeros in such a way that stability is reached. It is important to note that for a stable system with 60 degree of phase margin and an input signal bandwidth of 9.6 kHz, a resulting loop gain of 10 and a system delay of 400 ns was achieved.

The latency of the digital process and the signal processing time required for the DACs and ADCs characterize contributions to that delay. When comparing the input signal against the feedback signal this phase shift becomes critical. Similarly, aging, temperature fluctuations and non-linearities of the up and down converters and the PA contribute with phase shift [5]. To cope with this problem first, the phase shift has to be detected, and second it has to be corrected. A digital automatic phase detection [6] require two dividers, two look-up tables and one comparator. However, dividers are complex arithmetic units, and a look-up table requires a large amount of area when the bit length increases beyond 8 bits. In an analog automatic phase alignment [4] (Figure 2), the phase detection is obtained from

$$QI' - IQ' = \kappa_1 \kappa_2 sin(\theta - \theta') \tag{1}$$

where κ_1 and κ_2 are the magnitude of the input and feedback signals respectively. In comparison with [6] the arithmetic operations are simpler and the resulting equation (1) is monotonic over the range $-\frac{\pi}{2} < \theta - \theta' < \frac{\pi}{2}$. Additionally no memory elements are required.

One efficient mechanism to accumulate the phase difference in such a way that, in the steady state, the error signal is reduced, is by a linearized model as in Figure 3 [7] . This figure shows a model for the phase regulation loop. The error transfer function is given by

$$\theta_{error}(s) = \frac{s \cdot (\theta(s) + Phase\ distortion(s) + Drift(s))}{(s + C_0 e^{-Ts})} \tag{2}$$

where e^{-Ts} model the system delay in the loop and C_0 is an integration constant. Assuming that the input, phase distortion and drift signals are ramp signals with slope equal to ω_{in}, ω_{Pd} and ω_{Dr}, respectively, the steady-state phase error is found applying the final value theorem as

$$\begin{aligned} \lim_{t\to\infty} \theta_{error}(t) &= \lim_{s\to 0} s \cdot \theta_{error}(s) \\ &= \frac{\omega_{in} + \omega_{Pd} + \omega_{Dr}}{\kappa_1 \kappa_2 C_0} \end{aligned} \tag{3}$$

To reduce the phase error, C_0 must be higher than the sum of the input, the phase distortion and the drift signal frequencies:

$$C_0 \gg 2\pi \frac{f_{in} + f_{Pd} + f_{Dr}}{\kappa_1 \kappa_2}. \tag{4}$$

3. DIGITAL IMPLEMENTATION

3.1. Datapath

The digital implementation consist of two main blocks: the datapath block and the control block, as shown in Figure 4. The datapath includes all the logic for the arithmetics operations: the comparators to compute the I_{error} and Q_{error}, the phase detection and the integrator filter which provides the angle value for the CORDIC rotation, the CORDIC in vectoring mode to compute the magnitude and adder to compute the absolute value. The comparator is an adder that computes I_{error} and Q_{error}. It adds rather than subtracts the input and feedback signals as the feedback signal is already 180 degrees shifted due to the inversion of the PA. The selection of CORDIC for the implementation is due to the low power requirements for the digital circuit as well as the available system delay.

The implementation of (1) requires two multipliers and one comparator. For the digital integrator the most practical implementation is from its analog counterpart by means of the bilinear transformation [8], where a mapping from the s-plane to the z-plane is performed with

$$H(z) = \frac{C_0}{s}\Big|_{s=\frac{2}{Ts}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)} \tag{5}$$

The discrete transfer function H(z) is given by

$$H(z) = \frac{C_0 T_s}{2}\left(\frac{1+z^{-1}}{1-z^{-1}}\right) \tag{6}$$

where T_s is the sampling frequency. The realization of the filter, in transposed direct form II, is shown in Figure 5.

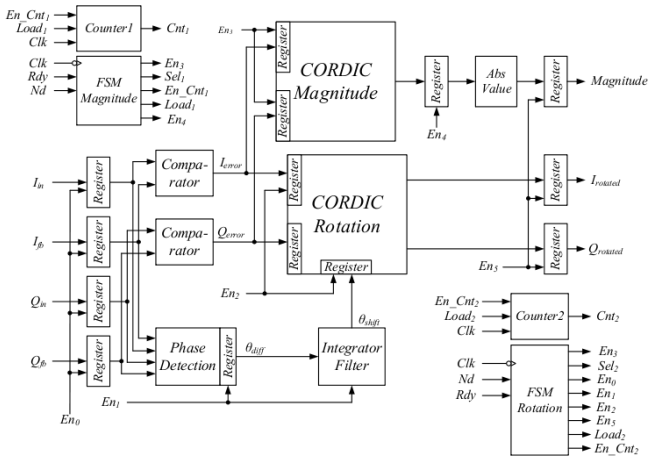


Fig. 4. Architecture realization of digital block.

The phase shift correction is carried out by a counter-clockwise rotation of the quadrature signals

$$\begin{pmatrix} I_{rot} \\ Q_{rot} \end{pmatrix} = \begin{pmatrix} cos(\Delta\theta) & sin(\Delta\theta) \\ -sin(\Delta\theta) & cos(\Delta\theta) \end{pmatrix} \cdot \begin{pmatrix} I_{error} \\ Q_{error} \end{pmatrix} \quad (7)$$

The matrix product (7) is implemented by means of a CORDIC algorithm in circular rotation mode [9]. In total a folded CORDIC implementation requires three adders, two barrel shifters and one small look-up table. In this implementation we decompose the rotation angle into smaller partial rotations of predefined angles in such a way that the rotation through each predefined angle can be accomplished with shift-and-add operations

$$I_{i+1} = I_i - \sigma_i \cdot I_i \cdot 2^{-i} \quad (8)$$

$$Q_{i+1} = Q_i + \sigma_i \cdot Q_i \cdot 2^{-i} \quad (9)$$

$$\theta_{i+1} = \theta_i - \sigma_i \cdot tan^{-1}(2^{-i}) \quad (10)$$

in which $I_0 = I_{error}$, $Q_0 = Q_{error}$, $\theta_0 = \theta_{shift}$ and σ_i is computed in such a way that θ_{i+1} tends to zero.

In a folded implementation of the CORDIC, each partial rotation takes one clock cycle and the total operation depend on the amount of precision bits required

$$I_{rot} = I_{scaling} \cdot I_{N-1} \quad (11)$$

$$Q_{rot} = Q_{scaling} \cdot Q_{N-1} \quad (12)$$

$$\theta_{rot} = 0 \quad (13)$$

where

$$I_{scaling} = Q_{scaling} = \frac{1}{\prod_{i=0}^{N-1} \sqrt{1 + \sigma_i^2 \cdot 2^{-2i}}} \quad (14)$$

and N is the number of steps or micro rotations. When the CORDIC is implemented in radix-2, σ_i can take only two values, -1 or 1, which means that $I_{scaling}$ and $Q_{scaling}$ are constant with the value

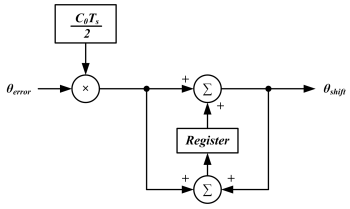


Fig. 5. IIR in transposed direct form II.

$$I_{scaling} = Q_{scaling} = 1.646760258 \quad (15)$$

In order to recover the envelope, the value of the magnitude which drives the EER is required. As the signals I and Q are perpendicular, we applied Pythagoras' theorem.

$$Magnitude = \sqrt{I_e^2 + Q_e^2} \quad (16)$$

As (16) shows, two multipliers or two squarers and one square rooter are required. The magnitude is implemented by means of a CORDIC algorithm in circular vectoring mode [9] in which $I_0 = I_{error}$, $Q_0 = Q_{error}$ and σ_i is computed in such a way that I_{i+1} tends to zero

$$I_{i+1} = I_i - \sigma_i \cdot I_i \cdot 2^{-i} \quad (17)$$

$$Q_{i+1} = Q_i + \sigma_i \cdot Q_i \cdot 2^{-i} \quad (18)$$

After N iterations the value of the magnitude is computed as

$$Magnitude = Q_{mag} = Q_{scaling} \cdot Q_{N-1} \quad (19)$$

$$I_{mag} = 0 \quad (20)$$

where $Q_{scaling}$ is given by (14). The CORDIC requires much less area than a square rooter, although with the penalty of longer latency. However, as the input bandwidth of the examined system was bound at 9.6 kHz, increased latency did not limit the system operation. In the CORDIC system, the value of the magnitude has to be corrected in sign due to the limited range of the CORDIC in vectoring mode. The absolute value is obtained by xoring the magnitude with its sign and adding 1 to the less significant bit.

3.2. Control blocks

Two finite state machines (FSMs) are implemented. One generates the CORDIC rotation control signals and the other generates the CORDIC magnitude control signals. Two 4 bits binary counters are used to keep track of the iteration steps of the CORDICs.

3.3. Optimization

It was shown in (4) that C_0 has to be much higher than the information signal bandwidth in order to reduce the phase

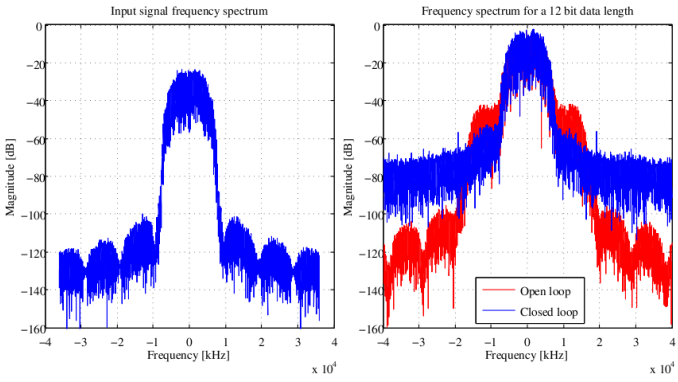
shift error. For a sampling frequency of 633 kHz, $\frac{C_0 T_s}{2}$ must be higher than 0.048; this condition is fulfilled by choosing $\frac{C_0 T_s}{2} = 0.0625$. The multiplication can be substituted by a 4 bits wired right shift. In general, the CORDIC implementation scales the output values, and usually that scaling factor has to be removed (by means of a division or multiplication). However, as the digital block is part of a loop it can contribute with gain. To this end each CORDIC contributes with a factor of 1.647 to the loop gain.

4. RESULTS

Simulations were carried out with an input bitstream of 19.2 Kbps, modulated in $\pi/4$-DQPSK. As the results indicate, 12 bits are required for a proper error computation of the quadrature signals. The frequency spectrum for the input signal and open and closed loop system is illustrated in Figure 6 and Figure 6b, respectively. In both, open and closed loop system, 20 dB amplification can be observed. Additionally, the closed loop achieves a distortion attenuation close to 20 dB with respect to the open loop. The design was implemented in the Xilinx Spartan3 X3s50-4tq144 FPGA. Table 1 shows the logic utilization and distribution. The minimum period achieved was 11.988 ns with a latency of 180 ns, and total power dissipation of 33.31 mW, running at 83.3 MHz clock frequency. Figure 7 shows the post place and route floor-plan and routing.

5. CONCLUSIONS

Mixed-signal Cartesian feedback proves to be an efficient linearization method for a stable system with sufficient phase margin. Such a feedback improves linearity when provided with adequate amount of loop gain. As the results obtained indicate, the use of the CORDIC algorithm proves to be a simple, low-power and robust solution, for the low bandwidth input signal.

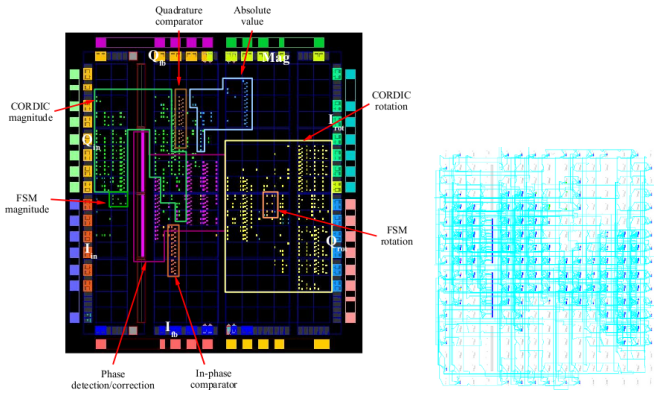


(a) Input signal spectrum (b) Output spectrum

Fig. 6. Frequency spectrum results.

Table 1. FPGA logic utilization and distribution.

Logic Utilization	Used	Available	Percentage
Number of Slice Flip Flops	126	1,536	8%
Number of 4 input LUTs	428	1,536	27%
Number of MULT18x18s	2	4	50%



(a) Post P&R floorplan (b) Routing

Fig. 7. FPGA implementation.

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