4. Comparison with the state-of-the-art CMOS SPADs

In general, deep-submicron SPADs have many advantages such as smaller pixel size, better timing resolution, larger array, higher speed, and higher fill factor. At the same time, however, there are also some disadvantages: lower and narrower PDP as well as higher tunneling noise due to higher doping concentrations. In order to compare performance of the proposed SPAD fabricated in 140-nm SOI CMOS technology to the literature in similar technology nodes, we restricted our attention to all reported substrate-isolated SPADs implemented in a feature size smaller than 250 nm [4, 13–18]. Consequently, SPADs fabricated in 350-nm CMOS technology are excluded in this comparison, although they exhibit good performance [19–21]. The reason for ruling out non-substrate-isolated SPADs is that they are not suitable for array configurations and for integration with electronic circuits in the same substrate due to high optical crosstalk and electrical interference from digital circuits [4, 22, 23].

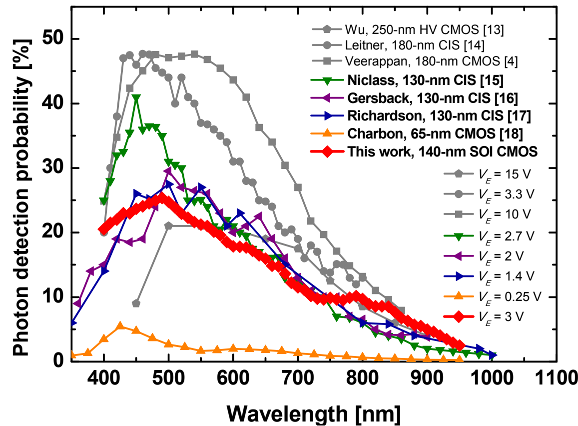

Fig. 8. SPAD-performance comparison: PDP.

Figure 8 shows a PDP-performance comparison. The SPAD reported by Veerappan *et al.* shows a high and wide PDP profile due to the wide depletion region using a deep N-well (DNW) having a lower doping concentration and very high excess bias voltage [4]. Leitner *et al.* and Niclass *et al.* also reported SPADs providing relatively high PDP because of a retrograde DNW and optimized dielectrics for optical detection, respectively, supported by the CMOS image sensor (CIS) technologies [14, 15]. Compared to other CMOS SPADs, the SOI CMOS SPAD exhibits medium PDP at short wavelengths but overperforms most SPADs in the literature above 750 nm.

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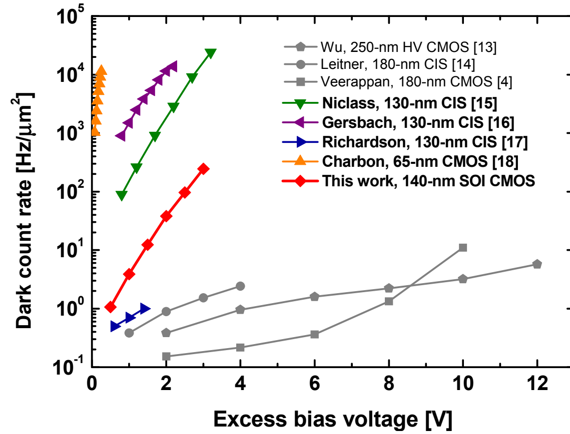

Fig. 9. SPAD-performance comparison: area-normalized DCR.

Figure 9 presents a DCR-performance comparison with the state-of-the-art CMOS SPADs. The SPADs fabricated in feature sizes larger than 180 nm tend to show better DCR performance. This is generally attributed to the fact that advanced CMOS technologies use narrower depletion widths and higher doping levels, which in turn cause higher band-to-band tunneling dark counts. Richardson *et al.* achieved low DCR using a low-doped P-well/retrograde DNW junction in the 130-nm CIS technology [17]. Compared with the similar-structure SPADs, which are based on P^+/N-well or N^+/P-well junctions, the DCR of the SOI CMOS SPAD is better than that of other SPADs implemented in 130-nm or 65-nm technologies. The state-of-the-art comparison of SPADs in terms of peak PDP and DCR is presented in Fig. 10.

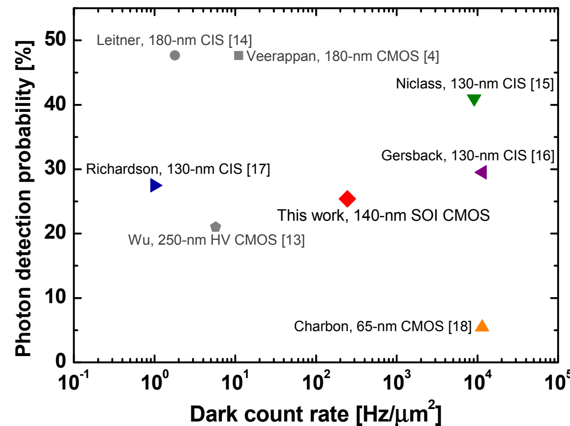

Fig. 10. SPAD-performance comparison: peak PDP vs. area-normalized DCR.

The performance of the SPAD implemented in the standard 140-nm SOI CMOS technology reported in this paper is summarized in Table 1. In addition, it reports a performance comparison with substrate-isolated SPADs fabricated in advanced CMOS technologies (140-nm technology nodes and below).

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Table 1. Performance summary and comparison with substrate-isolated SPADs fabricated in advanced CMOS technologies (140-nm technology nodes and below)

	This work	[15]	[16]	[17]	[18]
Technology	140-nm SOI CMOS Technology	130-nm CMOS Imaging Process	130-nm CMOS Imaging Process	130-nm CMOS Imaging Process	65-nm CMOS Technology
PN junction GR structure	P^+/N-well P-well GR	P^+/N-well P-well GR	P^+/N-well P&STI GR	P-well/DNW virtual GR	N^+/P-well N-well GR
Active area (diameter)	113.1 μm^2 (12 μm)	87.5 μm^2 (10 μm)	58 μm^2 (8.6 μm)	50 μm^2 (8 μm)	56 μm^2 (8 μm)
Shape	Circular	Octagonal	Circular	Circular	Octagonal
V_B	11.3 V	9.7 V	9.4 V	14.4 V	9.1 V
V_E	3 V	2.7 V	2 V	1.4 V	0.25 V
DCR (@RT)	27.6 kHz 0.24 kHz/μm^2	800 kHz 9.1 kHz/μm^2	670 kHz 11.6 kHz/μm^2	50 Hz 1 Hz/μm^2	640 kHz 11.4 kHz/μm^2
PDP peak	25.4% (@490 nm)	41% (@450 nm)	30% (@500 nm)	28% (@500 nm)	5.5% (@425 nm)
PDP @850 nm	7.7%	3.8%	4.2%	5%	0.5%
Afterpulsing probability	< 0.1% (@200-ns dead time)	n.a.	< 1% (@180-ns dead time)	0.02% (@100-ns dead time)	< 1% (@5-μs dead time)
Timing jitter	65 ps (@405 nm)	144 ps (@637 nm)	125 ps (@637 nm) (@V_E = 1 V)	200 ps (@470, 815 nm)	235 ps (@637 nm) (@V_E = 0.4 V)

DNW: deep N-well, GR: guard ring, V_B: Avalanche breakdown voltage, V_E: Excess bias voltage, RT: room temperature

5. Conclusion

We presented the first SPAD fabricated in standard SOI CMOS technology. The SPAD has been simulated, fabricated, and fully characterized in relation to the literature. Despite relatively high doping concentrations and higher defectivity of the SOI wafer, the realized SPAD has a DCR of 1.1 Hz/μm^2 at 0.5 V and 244 Hz/μm^2 at 3 V of excess bias, which is comparable to or better than DCR of similar-structure SPADs, based on P^+/N-well or N^+/P-well junctions, fabricated in advanced bulk CMOS technologies. The SOI CMOS SPAD achieves a peak PDP over 25% at 490-nm wavelength, along with enhanced PDP performance at long wavelengths due to the interface between silicon and BOX layers that acts as an optical cavity. With a dead time longer than 200 ns, the SPAD exhibits a remarkably low afterpulsing probability of less than 0.1%, and moreover it shows an excellent SPTR of 65-ps FWHM. The SPADs based on standard SOI CMOS technology will enable to provide future 3D-integrated image-sensor solutions.

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