A Structure of an Image Sensor Operating at 1 Gfps

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Introduction. "In-pixel Storage Image Sensor" with the idea of storing the image signals inside a pixel has been developed for ultra high speed imaging. In 2002, Etoh et all [1] achieved the practical frame rate of 1Mfps based on the slanted linear CCD storage design's concept. The highest frame rate of a CCD image sensor is 16.7 Mfps up to now. In this paper, an image sensor structure for image capturing with a frame interval less than one nano-second is proposed for applications to scientific and engineering fields requiring ultra-high-speedimaging, such as fluorescence lifetime imaging microscopy (FLIM), dynamic pressure sensitive paint imaging (DPSP), imaging of deformation of protein crystals, etc. The image sensor named as NanoSIS is taped out and under fabrication.

Structure. A wafer with n-/p- double epi-layers creates a high electric field to reduce travelling time of photo-electrons generated by incident photons to the back side to the front side of the pixel as shown in Fig. 1. Three-layer p-well makes a smoothly changing potential gradient towards the collection gates as well as protects the storage channel from the migration of generated electrons. Fig.2 shows the design of p-well in a pixel. It is known that the travelling time of the signal electrons from the back side to the front side is much shorter than the transferring time of the collected signal electron packets from the collection gate to the first memory element of the pixel. So, Multi-Collection-Gates (MCG) is proposed to achieve a frame rate of 1 Gfps [2]. Fig. 3 shows the design concept of a pixel. Collection area has five collection gates (A2 to A6) which will alternatively collect signal electrons while others are in transferring process. Another gate (A1) is used as a drain shuttering gate. So, the image sensor with this structure will be at least 5 times faster than the one with only 1 collection gate. Monte Carlo simulation is used to analyze the distribution of the traveling time of photo-electrons from the backside.

Operation. NanoSIS has two main operation modes: image capturing and readout mode. In the former mode, signal electrons generated by incident light travel from the backside to the front side and then to the collection area at center of each pixel thanks to the special wafer and the designed pwell layer as mentioned above. The assigned collection gate's (A4) voltage is higher than others to create a higher channel potential and attract electrons into it. A storage gate (B4) automatically collects and accumulates the charge from the collection gate thanks to its slightly higher potential. When image capturing process is done (5 consecutive frames has been already stored in all 5 storage gates), the readout mode starts. The stored charge is transfered from the storage gate (B4) to the neighboring transfer gate (D4) through the barrier gate (C4) and then three-phase CCD transfer is processed to transfer it downwards. All signal charges stored in the storage gates are read out to outside the sensor after the readout process is repeated three times. The drain gate's (A1) is used to drain out all the unwanted image signals through the pixel's drain (B1) during the process of readout mode.

Driving circuit. To achieve the frame rate of 1Gfps, a driving circuit is proposed which comprises a ring oscillator (RO) with an XNOR circuit to each invertor of the RO. We named the driver circuit RO-XNOR[3]. The performance of RO-XNOR is evaluated by circuit simulation as shown in Fig. 4. A test chip of RO-XNOR driver is fabricated and evaluated.

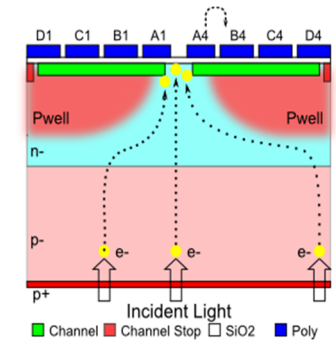

Fig.1 Travelling of electrons from backside to collection gate

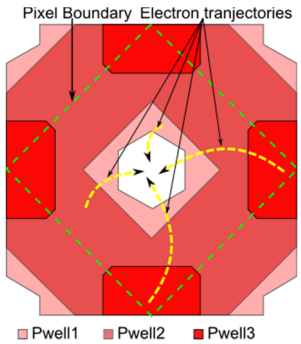

Fig.2 The Pwell Design

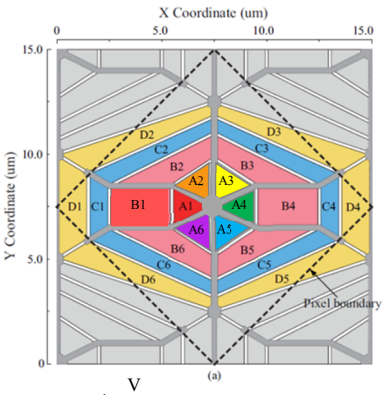

Fig. 3: Pixel Structure
A1: Drain gate;
A2-A6: Collection gates;
B1: Drain;
B2-B6: Storage gates;
C: Barrier gates;
D: Transfer gates

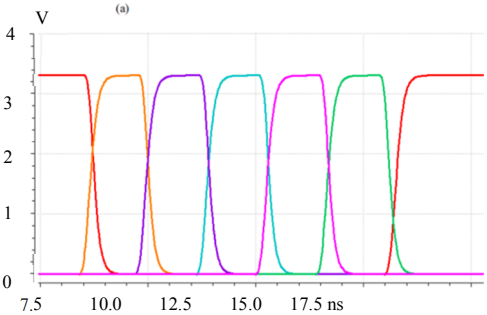

Fig. 4 Outputs of a RO-XNOR
– Driving voltage of the drain collection gate A1;
Driving voltages of multi-collection gates A2 to A6

References

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(3) C. Zhan et al., "Designing the localized drivers of a 3D 1Gfps image sensor family", *IISW 2015*.