

Layout Rules

UMC 90um 1P9M Process

QT-02/09,
v2011

Diffusion Layer (DIFF)

Minimum spacing and notch of DIFF to DIFF---0.14um

Minimum DIFF width for device---0.12um

Nwell Layer (NWEL)

- A: minimum Nwell width ---0.52um
- B: spacing and notch of Nwell to Nwell of equal potential ---0 or >=0.52um
- C: minimum NWEL enclosure of P+ DIFF ---0.21um
- D: minimum NWEL to P+ DIFF ---0.16um
- E: minimum NWEL enclosure of N+ DIFF ---0.16um
- F: minimum NWEL to N+ DIFF ---0.21um

NOTE: NWEL patterns must be orthogonal

Poly Layer (P01) —1

- A: minimum P01 width (gate length) for PMOS and NMOS---0.08um;
- B: minimum P01 overhang of DIFF (Poly1 end cap)---
 1. if Poly1 end cap area >=0.032um² ---0.14um
 2. if Poly1 end cap area <0.032um² ---0.18um
- C: minimum end cap P01 to related DIFF spacing ---0.06um
- D: minimum DIFF overhang of P01 gate ---0.15um

Poly Layer (P01) —2

- E: minimum spacing of P01 corner on field to DIFF
 1. P01 common run length with adjacent, parallel DIFF<=0.2um---0.06um
 2. P01 common run length with adjacent, parallel DIFF>0.2um---0.08um
- F: minimum spacing of parallel P01 gates ---0.16um
- G: minimum spacing and notch of P01 on field ---0.16um

N+ Implant Layer (NPLUS)

- A: minimum NPLUS width ---0.20um
- B: minimum NPLUS spacing and notch ---0.20um
- C: minimum NPLUS overhang of N+ DIFF for NMOS ---0.11um
- D: minimum NPLUS overhang of NMOS gate ---0.18um
- E: minimum overlap of NPLUS to DIFF to form N+ region ---0.16um

P+ Implant Layer (PPLUS)

- A: minimum PPLUS width
---0.20um
- B: minimum PPLUS spacing and notch
---0.20um
- C: minimum PPLUS overhang of P+ DIFF over Nwell
---0.11um
- D: minimum PPLUS overhang of PMOS gate
---0.18um
- E: minimum overlap of PPLUS to DIFF to form P+ region
---0.16

Metal 1 Layer (ME1)

- A: minimum ME1 width---0.12um
- B: minimum ME1 spacing and notch---0.12 um, but 0.18um for ME1 with width>0.70um; 0.34um for ME1 with width>2.8um
- C: minimum ME1 line end enclosure of Contact---0.04um
- D: minimum ME1 line end enclosure of Contact for 4 sides
---0.02um
- E: minimum ME1 line end enclosure of Contact---0.08um
(if ME1 width \leq 0.14um and the spacing of ME1 line end to 3 adjacent ME1 patterns \leq 0.14um-i.e. d1, d2 and d3 \leq 0.14um)

Contact Layer (CONT)

- Minimum DIFF enclosure of CONT---0.02um
- CONT must be within P01 or DIFF and not over gate area
- Minimum spacing of DIFF CONT to P01---0.08um
- Minimum P01 enclosure of CONT---0.02um
- Minimum CONT spacing if common run length \geq 0---0.16um
- Minimum spacing of P01 CONT to DIFF edge ---0.08um