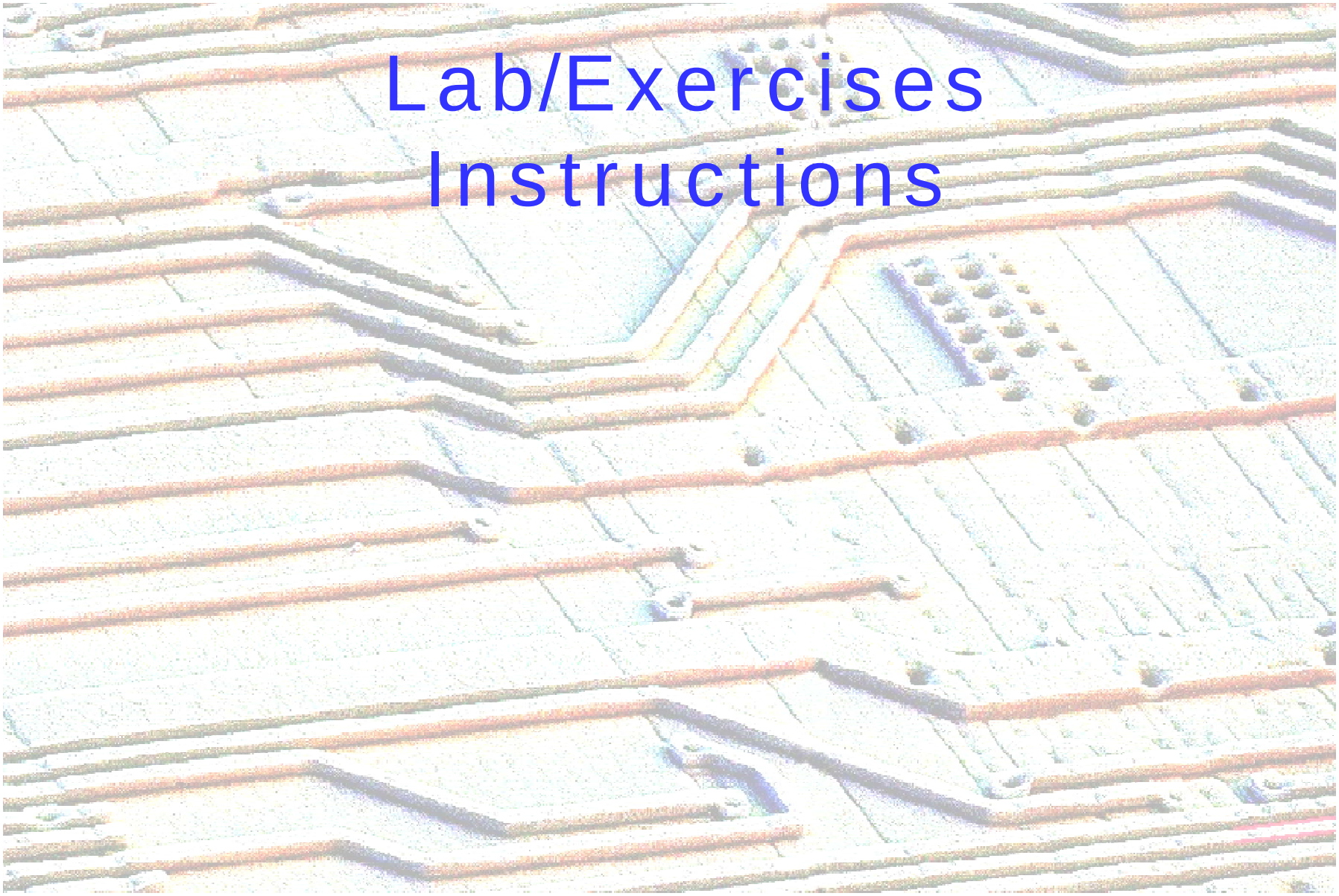


Lab/Exercises Instructions

Assignment 1: Spectre

Use Spectre for Rabaey Exercises 3.4 and 3.5

- **Spectre information/how to on course web site**
- **There are other ways to run Spectre, do as you see fit …**
- **Better to use Spectre than other simulator (Spice, ADS, …) which you may feel more familiar with – you need to learn Spectre anyway**
- **Hand-in 1 A4 with 4 annotated graphs on Thu 21/2 before class**
- **Write you names (as a team) on it**

- **Due date: Thu Feb 21**
- **Will not be graded, but will be checked. Need to pass**
- **We will provide feedback if necessary**

Assignment 2: Virtuoso

Virtuoso Layout Design and Schematic Driven Layout

- **Draw a PMOS transistor using Virtuoso**
- **Make sure it is DRC correct using Calibre**
- **See layout design rules (ppt/pdf on web)**
- **Design an inverter using Schematic Composer and Spectre Simulation**
- **Design Layout using Virtuoso Analog Design Environment (Schematic Driven Layout)**

- **Hand-out with extensive instructions is on course website**

- **Due date: Mon Feb 25**
- **Not to be graded, but will be checked. Need to pass**
- **We will provide feedback if necessary**

Assignments need to be Checked

- **You need to complete the assignments**
- **No grading – just pass/fail**
- **a serious attempt counts as pass,**
  not needed to have everything exactly correct and optimal
  (but it can give you satisfaction)
- **A non-serious attempt requires improvement**
- **We will try to give feedback, so that you know what is OK and what needs improvement**
- **Hand in to TA's when you are done ☺**
- **Ask TA's when you are stuck ☹**

TA Help

- **Lucho Gutierrez (TA),**
  Yuxin Yan (TA),
  Venkat Krishnaswami (PhD)
  Availability: see BB contact information

- **Might also come to lab in rush hours**

- **BB Forum – me and TA's will answer questions**

Logistics

- **Prepare yourself, form pairs**
- **Register pairs on BB -> groups -> sign up form**
- **Become familiar with linux, cadence**
- **Can only use computers in MSc lab Room LH 0.530 (ground floor of EWI low building, the long corridor)**
- **Instructions are posted on web, being augmented through the course**
- **Login using netid**
- **Door lock: see BB**
- **Use time slot registration sheets**
- **Odd/Even groups have priority on alternating days**

- **Next: example of Spectre way of working for exercise Rabaey 3.11**

Rabaey Exercise 3.11

11. [M, SPICE, 3.3.2] Problem 11 uses the MOS circuit of Figure 0.7.

a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). $V_{DD} = 2.5$ V.

b. Repeat *a* using SPICE.

c. Repeat *a* and *b* using a MOS transistor with $(W / L) = 4 / 1$. Is the discrepancy between manual and computer analysis larger or smaller. Explain why.

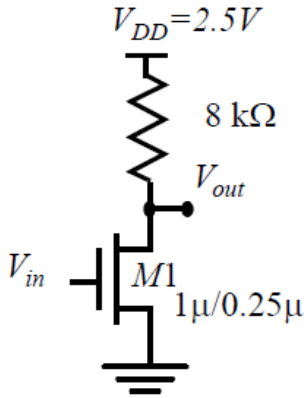
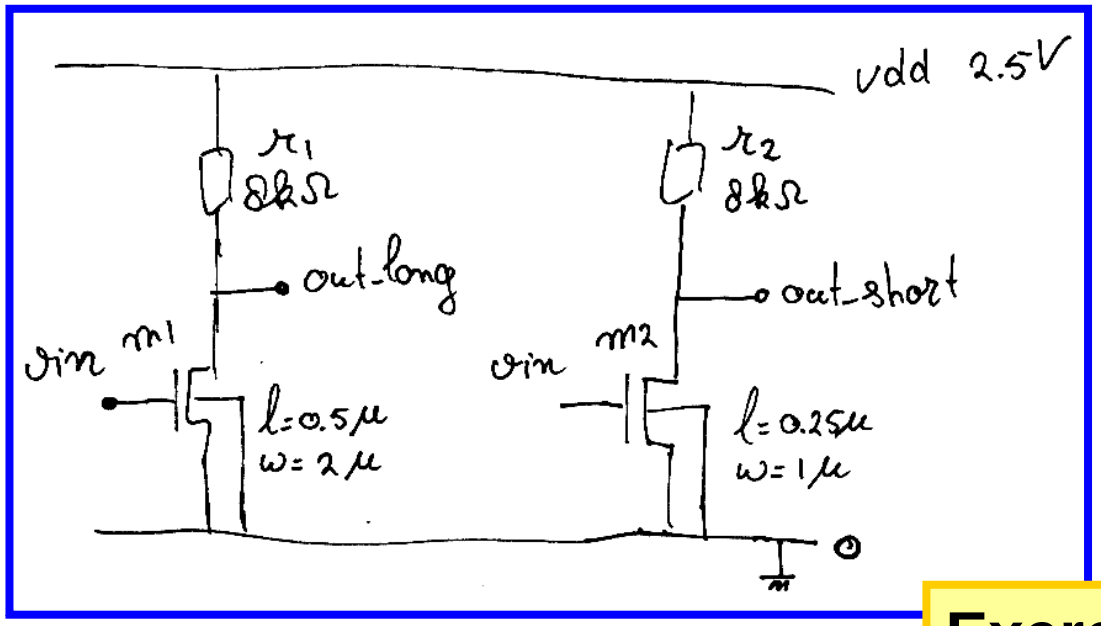


Figure 0.7 MOS circuit.



Simulation Example

- **Make sketch**
- **Assign node names**
- **Write file**
- **Add control statements**

Exercise 3.11

```
simulator lang=spectre
include "g25_scs.lib"
vdd (vdd 0) vsource dc=2.5
vin (in 0) vsource dc=2.5
r1 (vdd out_long) resistor r=8K
r2 (vdd out_short) resistor r=8k
m1 (out_long in 0 0) nmos l=0.5u w=2u
m2 (out_short in 0 0) nmos l=0.25u w=1u
Inputsweep dc param=dc dev=vin start=0 stop=2.5 step=0.1
save vin out_long out_short
```

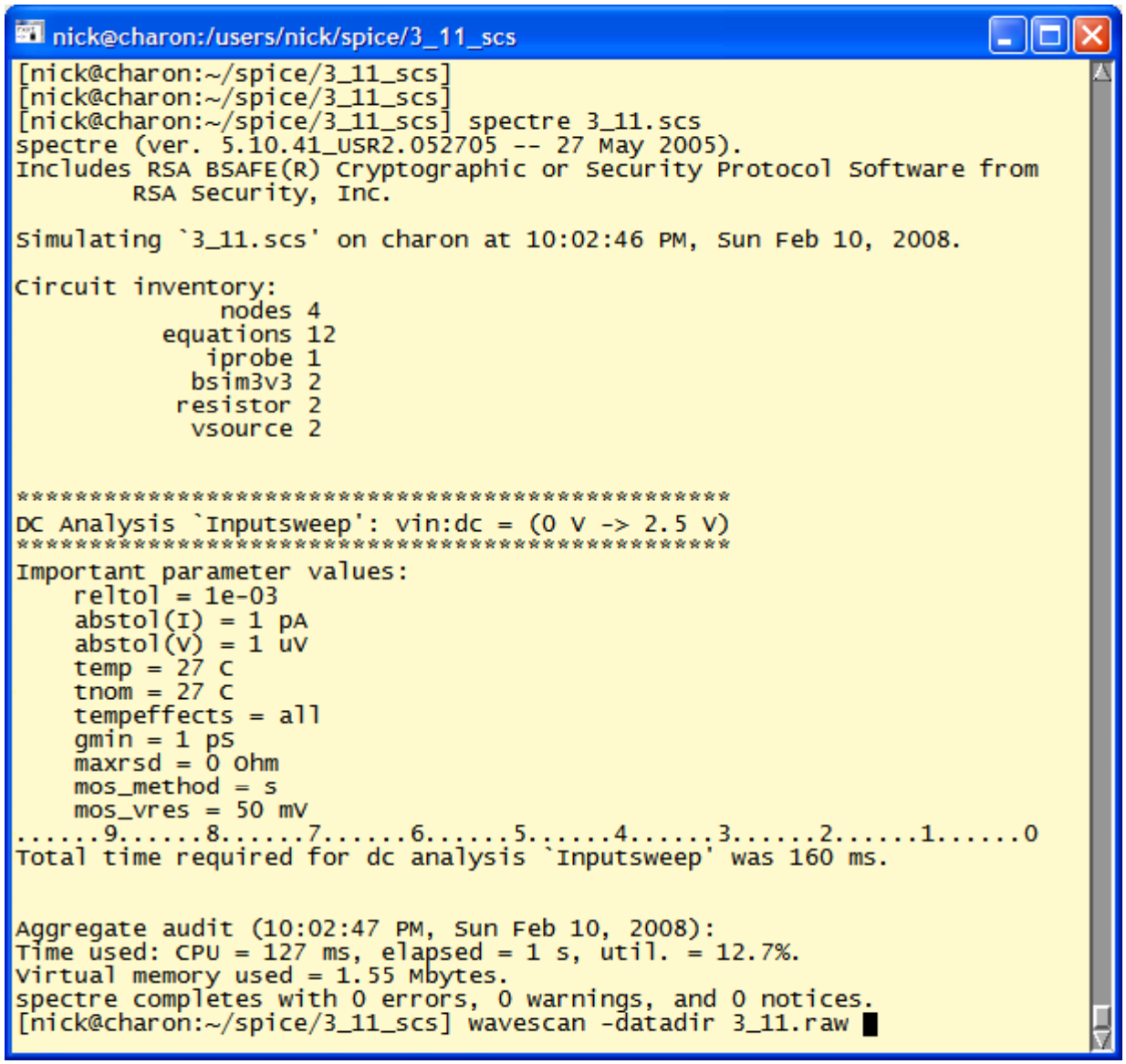
<- model doesn't allow l=1

250nm Spectre BSIM3 MOS Models

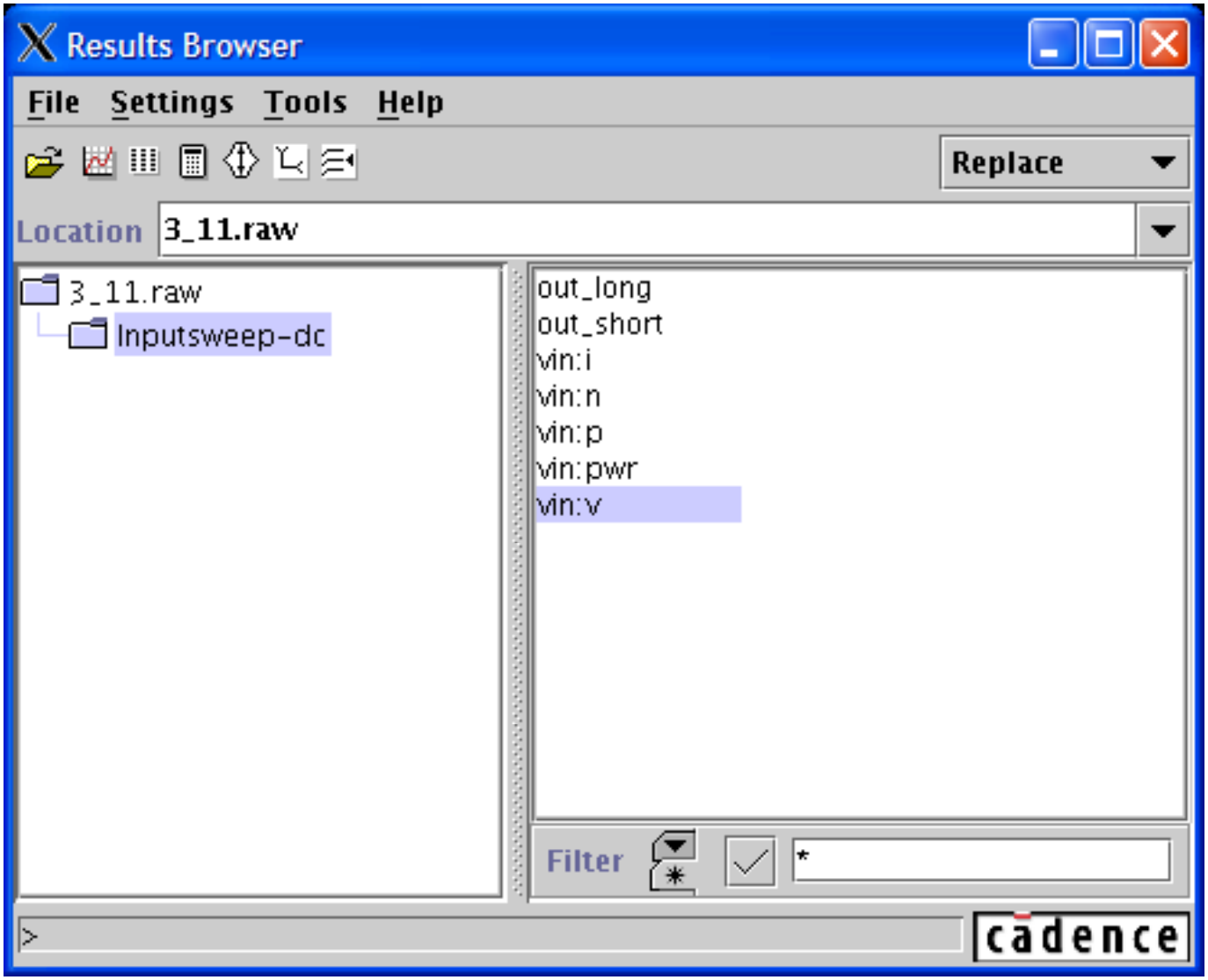
```
simulator lang=spectre
model nmos bsim3v3
+version=3.1
+type=n
+tnom    = 25              xl      = 3e-8
+xw      = 0               tox     = 5.8e-9
+xj      = 1e-07           nch     = 2.354946e+17   lln     = 1
+vth0    = 0.4321336       lvth1   = 2.081814e-08   wvth0   = -5.470342e-11
+pvth0   = -6.721795e-16   k1      = 0.3281252      lk1     = 9.238362e-08
... 60 lines deleted ...
+tlev    = 1               tlevc   = 1              js      = 1e-06
+jsw     = 5e-11
```

- **Similar for pmos device**

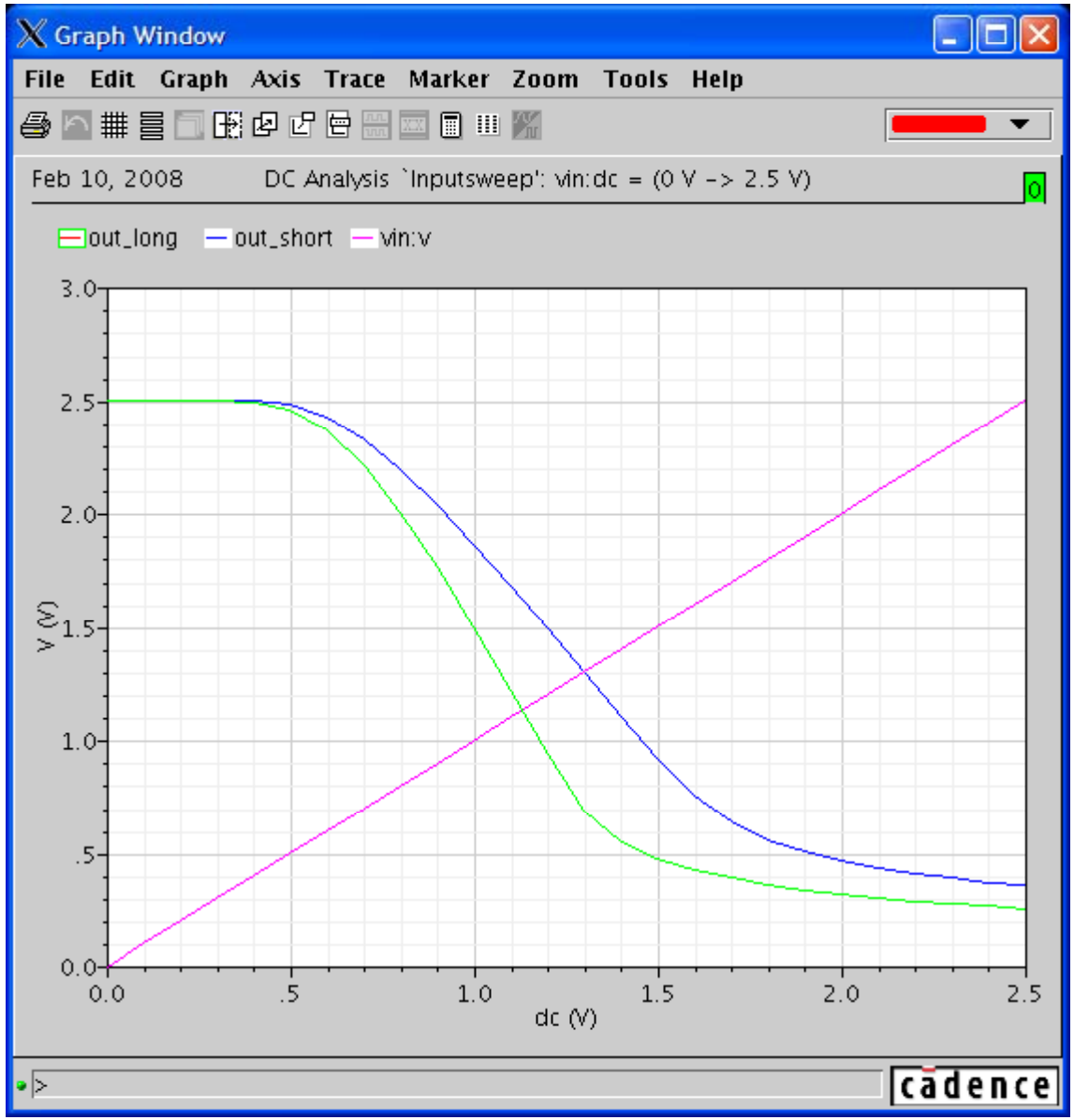
Spectre Terminal Interface



WaveScan Results Browser



WaveScan Graph Window



Exercise 3.4+3.5

4. [E, SPICE, 3.3.2] Using SPICE plot the *I-V* characteristics for the following devices.

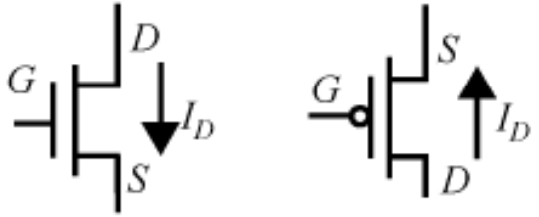


Figure 0.3 NMOS and PMOS devices.

a. NMOS $W = 1.2\mu m$, $L = 0.25\mu m$

b. NMOS $W = 4.8\mu m$, $L = 0.5\mu m$

c. PMOS $W = 1.2\ \mu m$, $L = 0.25\ \mu m$

d. PMOS $W = 4.8\ \mu m$, $L = 0.5\ \mu m$

5. [E, SPICE, 3.3.2] Indicate on the plots from problem 4.

a. the regions of operation.

b. the effects of channel length modulation.

c. Which of the devices are in velocity saturation? Explain how this can be observed on the *I-V* plots.

Tips for Ex 3.4, 3.5

- **Make 4 circuits, 1 for each of the cases 4a-4b**
- **Each circuit will have 6 transistors**
  - **All drains are connected, drain voltage to be swept from 0 to 2.5 V**
  - **All gates unconnected, different gate voltages: 0, 0.5, 1.0, 1.5, 2.0, 2.5 V**
- **Alternatively, use parameter sweeping instead of different layouts**
- **Plot each circuit in a separate graph, combine them on 1 page (word or latex)**
  - **Wavescan can *export png files*, looks better compared to screen dumps**