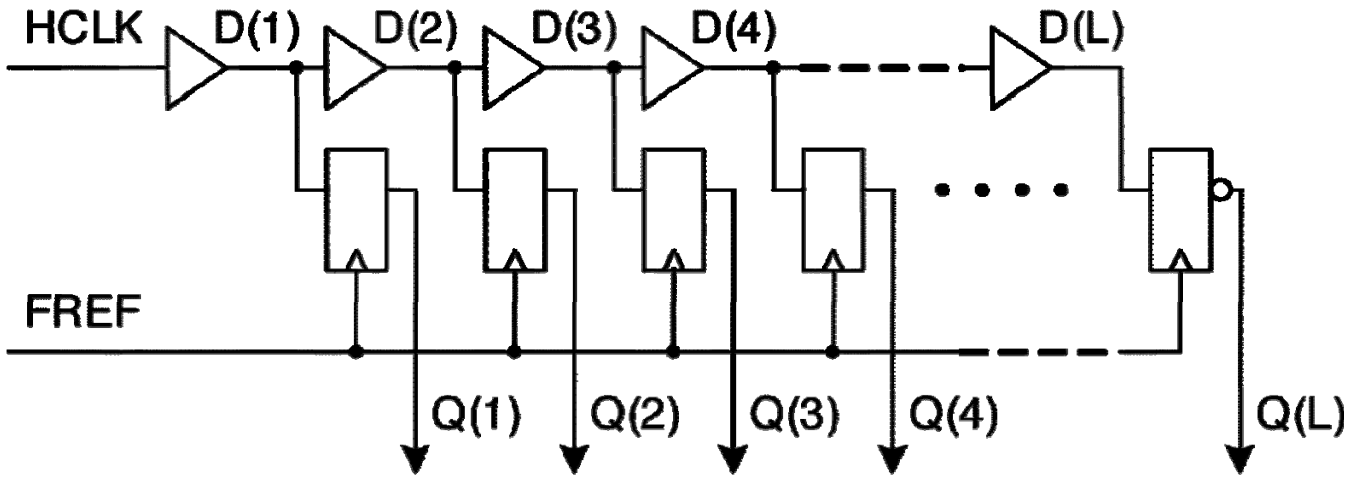
Project: Time to Digital Converter

- **Project specs updated on March 15th**
- **Believed to be final**

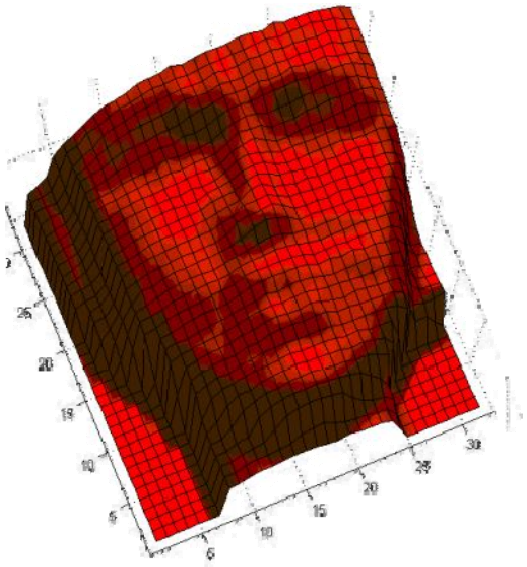
Changes:

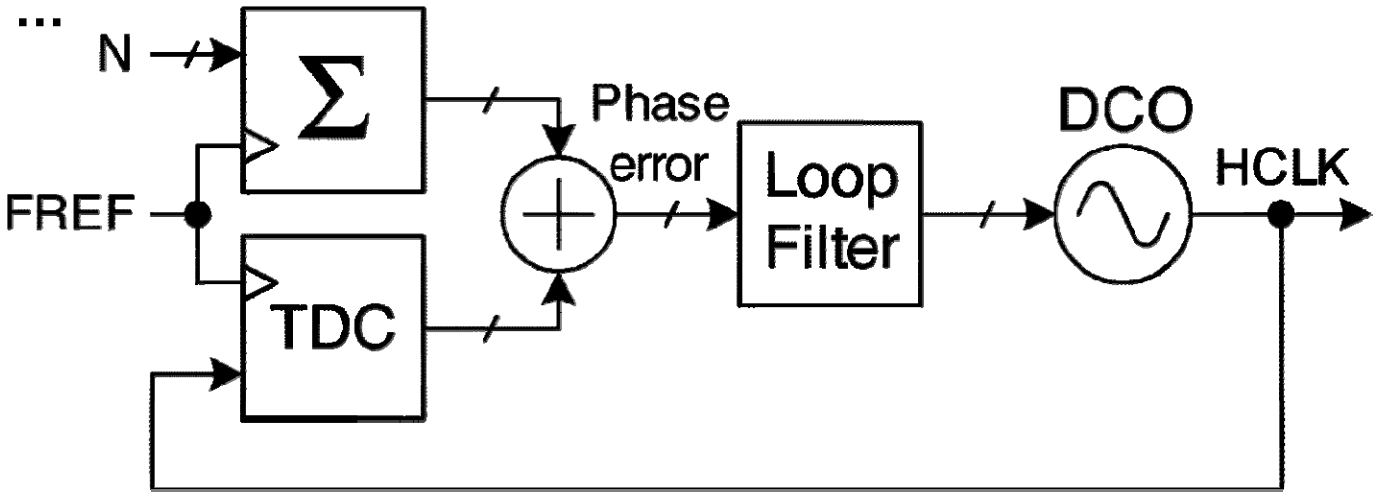
- **Reset signal added (Slide 10)**
- **FoM defined as Energy x Area x Resolution (Slide 15)**



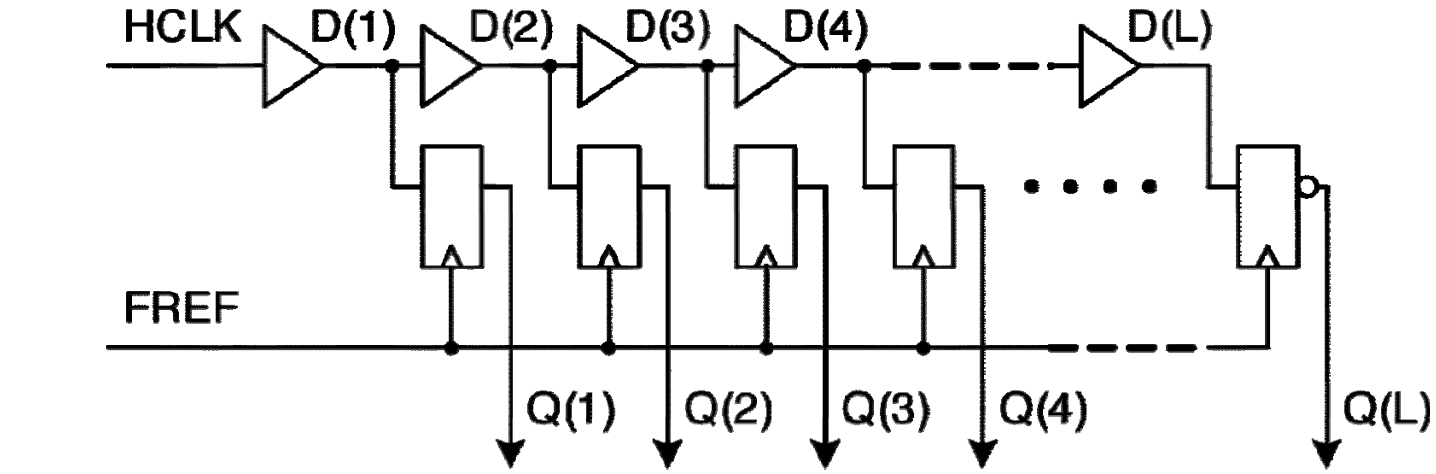
Applications

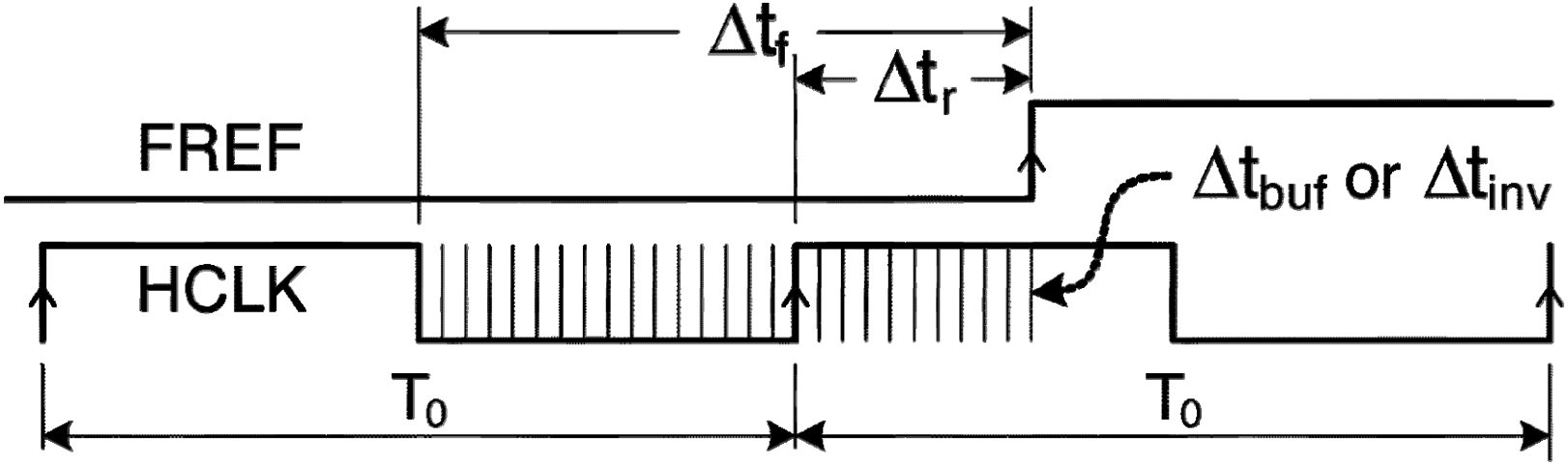
- **Instrumentation:**
  - **High Energy Physics**
  - **Astronomy / Space Science**
  - **…**
- **Time Resolved Cameras (Edoardo Charbon)**
- **Digital Frequency Synthesis (Bogdan Staszewski)**
- **…**

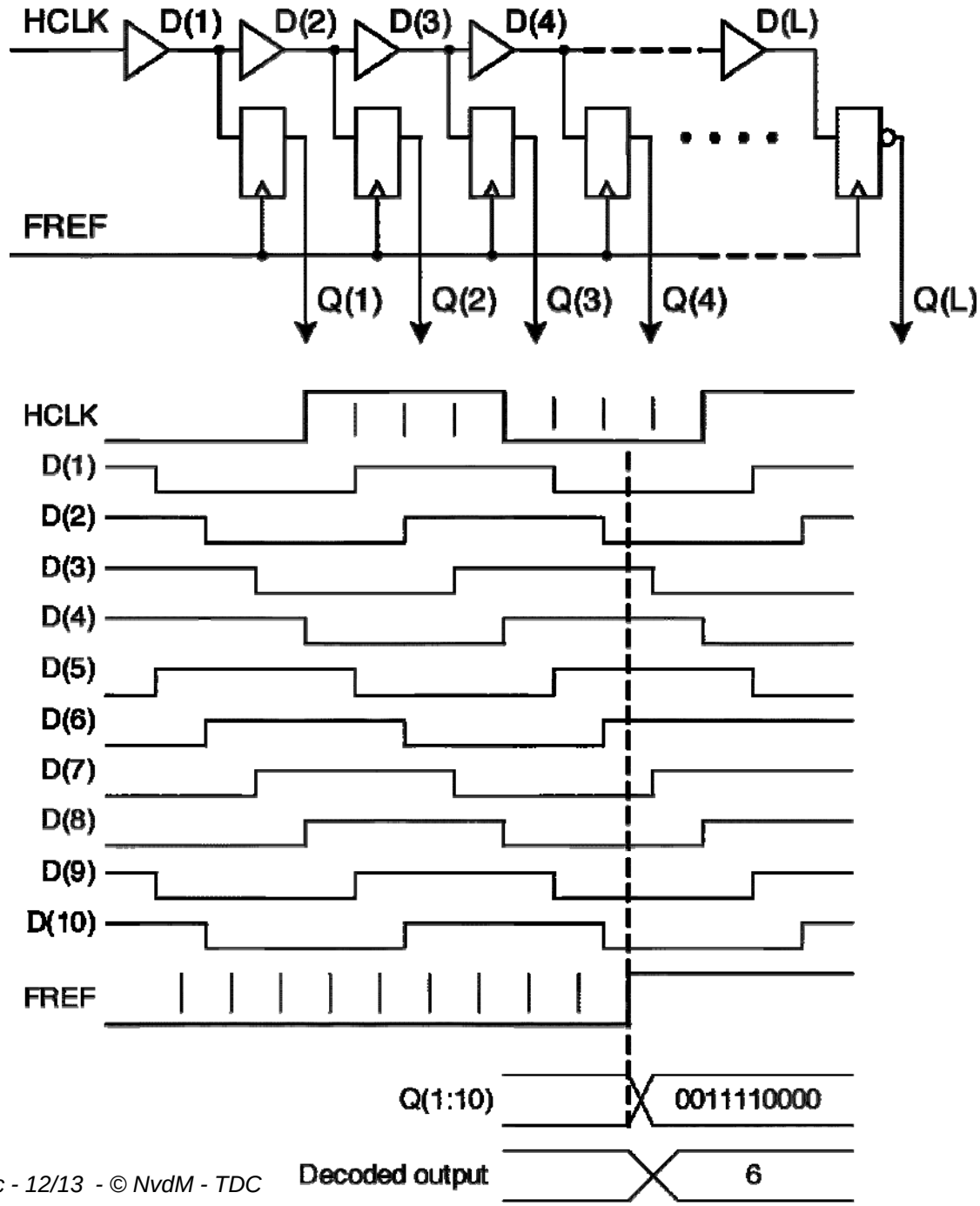




Project


HCLK
D(1)
D(2)
D(3)
D(4)
D(L)
FREF
Q(1)
Q(2)
Q(3)
Q(4)
Q(L)


Δtf
Δtr
FREF
Δtbuf or Δtinv
HCLK
T0
T0

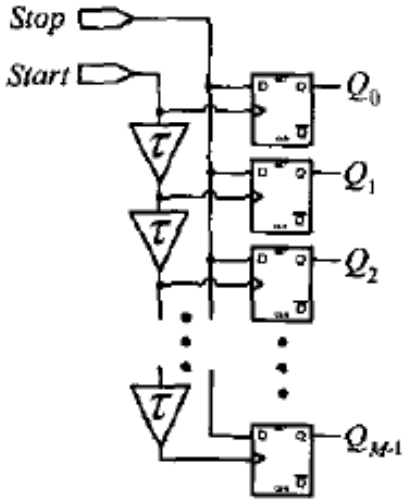

HCLK
D(1)
D(2)
D(3)
D(4)
D(L)
FREF
Q(1)
Q(2)
Q(3)
Q(4)
Q(L)
HCLK
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
D(7)
D(8)
D(9)
D(10)
FREF
Q(1:10)
0011110000
Decoded output
6

TDC Architectural overview

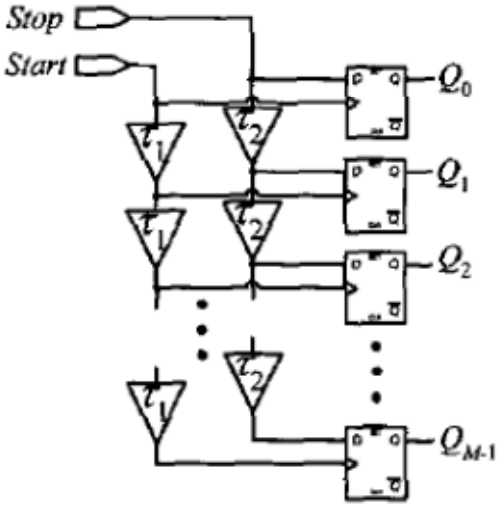
- **Sub-gate delay resolution realized by:**
  - **Delay line**
  - **Vernier delay line**
  - **Pulse-shrinking**
  - **Parallel delay elements**
  - **Delay amplification**
  - **Scrambling**
  - **Delay line with local passive interpolation**

Delay Line

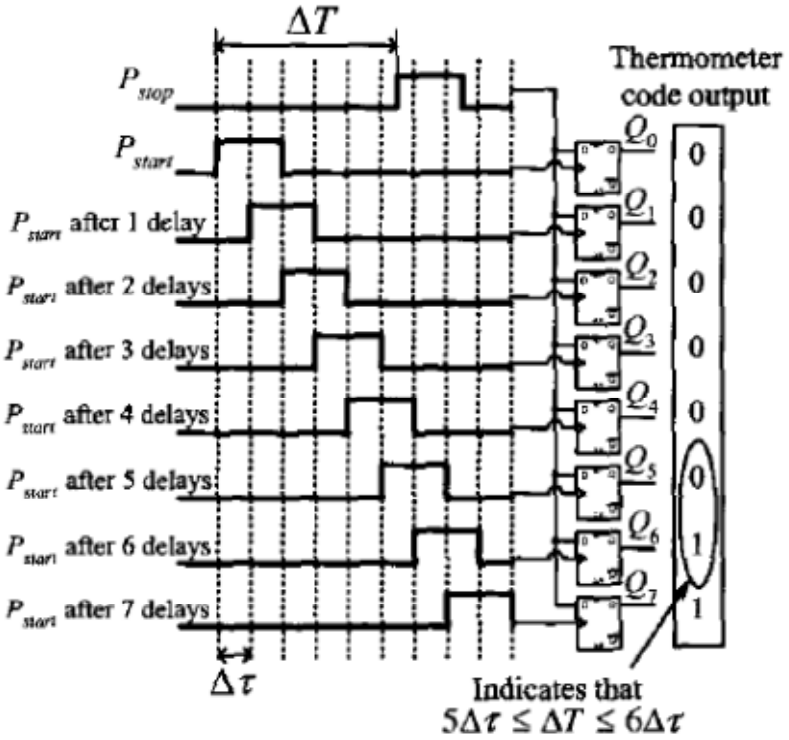
Single delay chain



Vernier delay chain



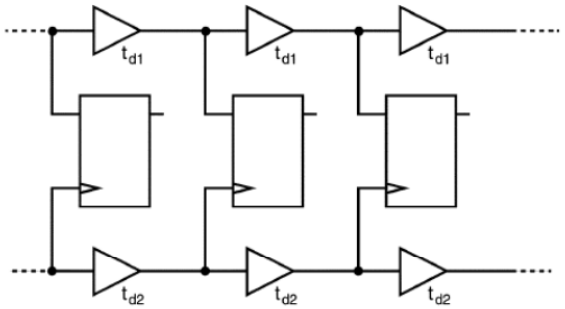
8-level delay chain



Pulse Shrinking TDC/Parallel Delay

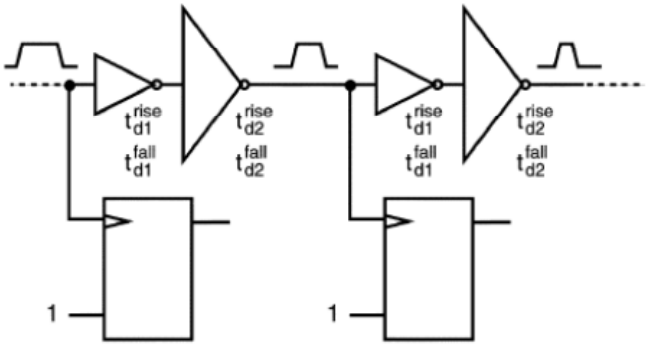
Vernier delay chain

R. Staszewski, JSSC ’04



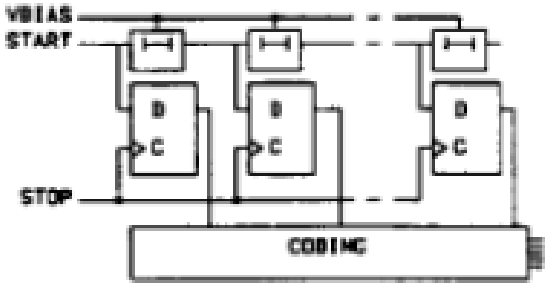
Pulse shrinking

P. Chen, TCAS-II ’00

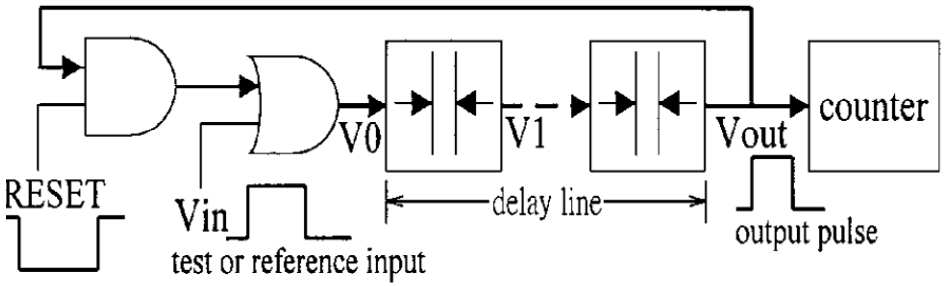


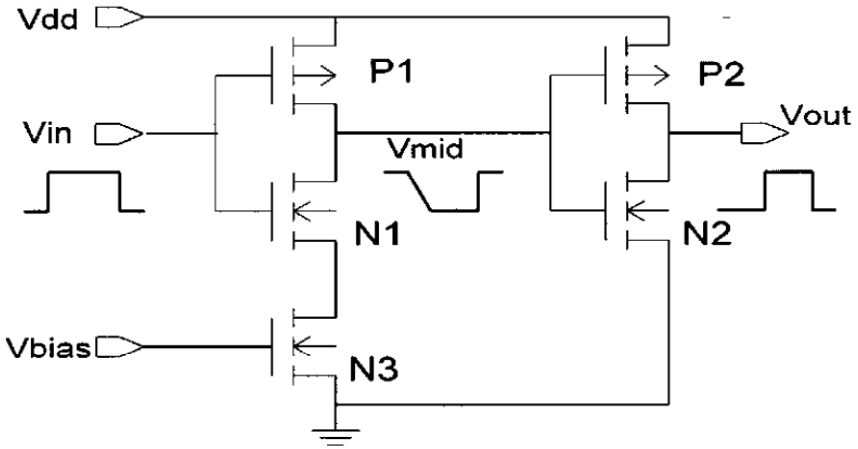
Parallel delay

Rahkonen, JSSC ’93



Pulse Shrinking TDC





- **Pulse is launched into inverter chain**
- **It becomes narrower on each iteration**
- **Count until it vanishes**

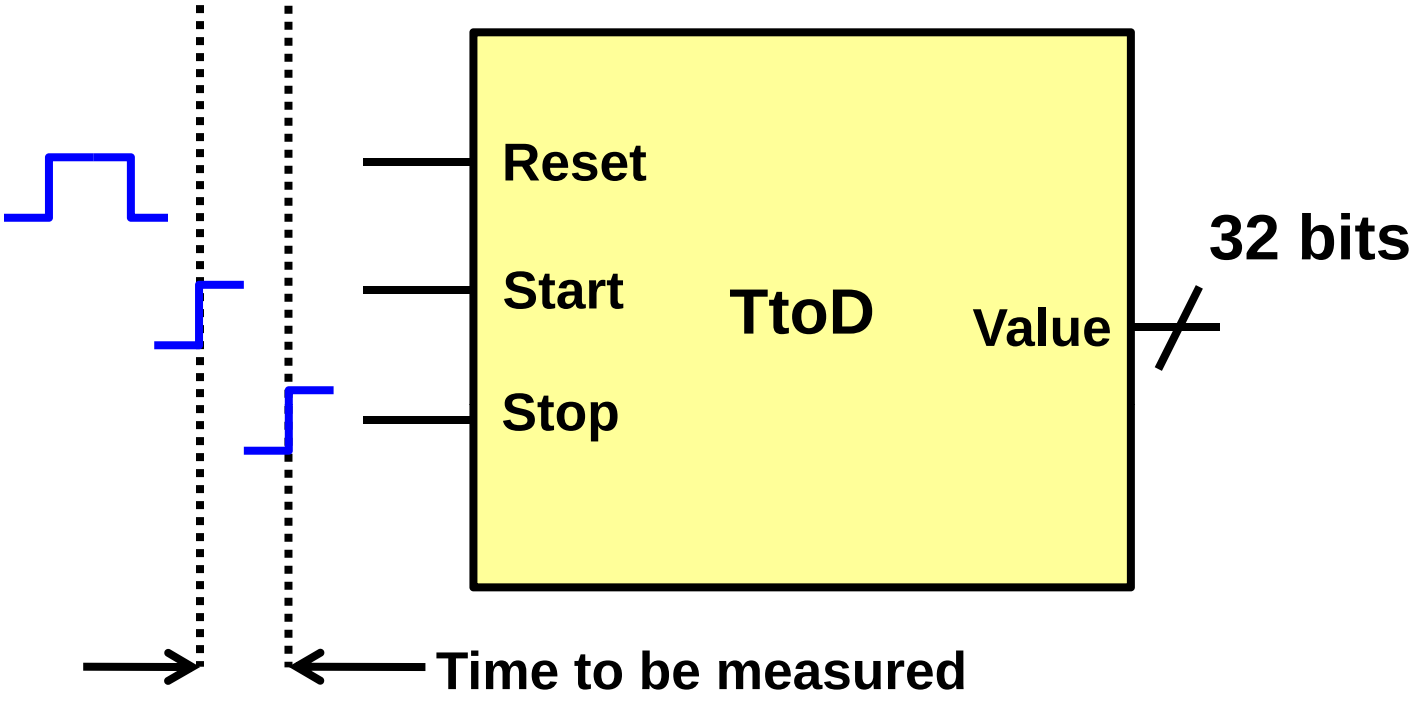
Project Requirements

(subject to minor changes)

- **5 bits – 32 steps – Vernier type or single delay line**
- **Better than 40 ps resolution (~~ref: unloaded inverter delay 26 ps~~)**
- **Other than that, you should design something that provides a good tradeoff between**
  - **Speed (timing resolution)**
  - **Area (to be measured in sum of transistor widths)**
  - **Power (average energy per conversion)**
  - **Sample rate (number of acquisitions per second)**
- **See subsequent slide on Design Tradeoffs**

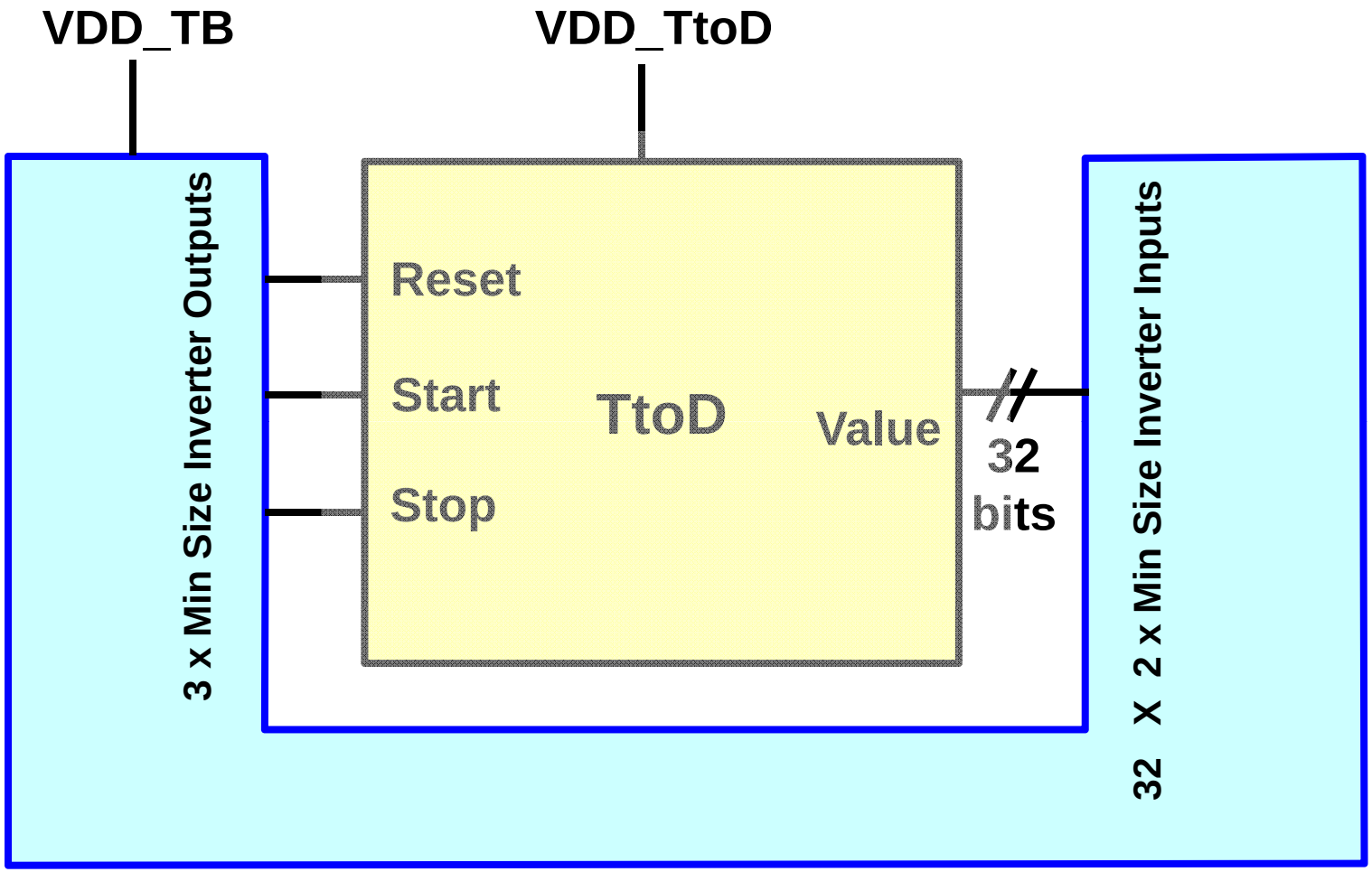
- **L_{min} = 80nm, W_{min} = 120 nm**
- **Supply voltage is variable (design specific – your choice)**
- **Circuit – Simulation – Spectre Simulation (No Layout)**

Top Level Architecture



- Start/stop architecture
- Binary output
- Range of time to be measured is
  0 – 2^5-1 times ***your*** specified resolution

Test Bench



- Test bench will be made available (about begin of april)
- Power/Energy of VDD_TtoD is measured

Design Tradeoffs

- Design is a tradeoff – design depends on application
- You should optimize one or more of the relevant metrics, possibly at the cost of others
- In the end, you should know and defend
  - what is good about your design,
  - what is less good
- Try to excel in one or more of
  - Speed (timing resolution)
  - Area (to be measured in sum of transistor widths)
  - Power (average energy per conversion)
- Acquisition rate is another relevant metric
- As long as you reach the 40 ps timing resolution

Design Robustness

- **Robustness of design:**
  it works independent of
  - **Process variations**
  - **Layout parasitics**
  - **Voltage and temperature conditions**
  - **Aging**
  - **…**
- **Full robustness aware design outside project scope**
- **But: limited corner analysis is necessary**
- **Details follow later,**
  also see subsequent slide on “process corners”

Process Corners

- **Because of manufacturing tolerances, I_D of different transistors differs even if voltages are same**
- **Some transistors are slowest (smallest I_D), some are fastest (highest I_D)**
- **Robustness of design is usually assured during simulation by accounting for different combinations of transistor speeds**
- **Example: all NMOS are slow, all PMOS are fast. This is called the slow/fast corner.**
- **Other "corners": Slow/Slow, Typical/Typical, etc.**
- **See wikipedia: process corners**

		NMOS		
		Slow	Typical	Fast
PMOS	Slow	S/S		F/S
	Typical		T/T	
	Fast	S/F		F/F

Award

- **Bonus point for top 20 % best results**
  - **1 bonus point for best 10 %**
  - **0.5 bonus point for next 10%.**
  - **Counts on overall grade, not just project grade**

- **Eligibility for bonus depends on all performance factors.**
  - ~~**Should excel in at least one performance metric (speed/power/area)**~~
  - **FoM ~ Energy x Area x Resolution**
    Resolution: t_{LSB} (time of least significant bit)
    Energy will be averaged over a number of conversions ranging from $1t_{LSB}$ to 31 t_{LSB}
  - **Average metric in FF and SS corner is ranked**
  - **Includes reporting, timeliness, presentation.**

Feel free to

- **Use any circuit style (Chapter 6)**
  - complementary CMOS, ratioed logic, DCVSL, pass-transistor logic, CPL, dynamic logic, … (No need to stick to style from book)
- **Any architecture**
- **Consider any known (or unknown ☺) technique to improve your metrics**
  - ckt level: body bias, sub-threshold logic, …,
  - design: automatic sizing, …

Deliverables

- **Midterm version of Report**
- **Project files**
- **Final Report**
- **Presentation files**

- **Symposium – present your design to expert panel, Q&A, details follow**

Midterm Report

- Describes target application
- Describes and motivates architecture choice in view of selected target application
- Give target specs of your design – based on preliminary modeling and simulations, including SS and FF corner
- Includes design of key circuit blocks
- Midterm report must become integral part of final report, not tacked onto it as an appendix
- Due: Mon Mar 18, upload via BB
- You get feedback in week of Mar 25
- We might give you a NO GO based on findings
- Later, you have to defend deviations from specs and architecture changes
- …

FAQ

Q: The project looks simple, because we don't have many degree's of freedom. Is that all we need to do?

A: Yes, but you should show

that you master the design process,
that you know what you do and why
that you can properly document the design
that you can properly present the design

Q: Can we use standard cells?

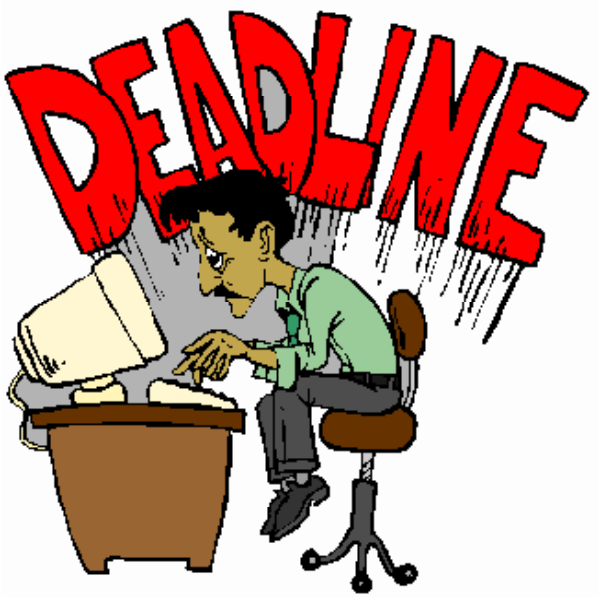
A: You cannot use a library –
you have to design all cells yourself.

Delivery Date

- **Midterm report**:
  Monday, March 18, 9:00 (week 3.6)
- **Design + Report + Presentation slides**:
  Wednesday, April 24, 9:00 (week 4.1)

- **Symposium tentatively week 4.3**

- **0.1 point penalty per day of late delivery**
  max 1 point penalty



Submissions

- **All reports: only pdf allowed**
- **Presentation: pdf or ppt**
- **Pack multiple files using zip or tar**
- **Naming scheme for each upload (doc and files): use group number and last names, see example:**
  11-lastname1-lastname2-midterm.pdf
  21-lastnamea-lastnameb-project.tar

Grading

- **Final grade 50/50% project/exam**
- **Need at least a 5 for either part, or result invalid**

50%	**Exam**	**Written exam**
30%	**Design**	**Correctness, creativity, elegance, robustness** **A correct design gives at least a 6.**
10%	**Presentation**	**Relevance, information, (presentation skills)**
10%	**Report**	**Midterm report is part of final report** **Relevance, information, documentation (design decisions) (brief, factual, clarity and ease of reading (!), documentation, not essay or paper)**

Bonus Points

- **Metric: Energy x area x resolution**
- **Average metric in FF and SS corner is ranked**
- **Bonus point for top 20 % best results**
  - **1 bonus point for best 10 %**
  - **0.5 bonus point for next 10%.**
  - **Added to overall grade, not just project grade**

Report and Presentation Guidelines

- **Target audience**

  your peer group of students, but when you just entered the MSc program at Delft University

- **Writing / Presentation objective**
  - **Document design, design choices**
  - **What, why, and how (and how not)**
- **Convince us that**
  - **You understand what you are doing and why**
  - **You are (becoming a) good academic engineer**

Report (Learning) Goals

- **To be considered as exercise for (thesis) writing**
- **Report needs to be improved until OK**
  - **First submission most important for grade**
- **Consider learning LaTeX**

Report Guidelines

- **Title page**
  (including admin data like names, email, student numbers, date, class, …)
- **Abstract – short summary of what you did, results, and not how you did it.**
- **Introduction – the project context**
  background of project, design requirements and expectations, project boundaries, project objectives
  overview of literature, background theory, state-of-the-art, … + intro to rest of report
- **Body of report – see next slide**
- **Conclusion**
  Includes summary of contributions, use evidence to support claims
  Don't introduce new information in conclusion
  Recommendations (if any) (for design or for class)
- **References – see subsequent slide**
- **Appendices**
  All value-adding material that would make main text too long

Body of Final Report

- **Design**
  - **Architecture of design, the design itself**
  - **the creative ideas of the design, what is special.**
  - **the cells used for the design and the sizes of transistors in every cell.**
  - **Important schematics, waveforms, …**
  - **the reason and/or methods to choose the specific cells, transistor sizes and system structure.**
- **Results**
  - **Overall simulation results, simulation settings**
  - **Power, VDD, transistor count figures, other relevant (design specific) statistics**
  - **Everything needed for demonstrating functionality and performance**

References

- **Proper citation is mandatory**
  - **All ideas that are not common knowledge and not new ideas by you should be cited**
  - **Science requires proper traceability of ideas**
  - **All sources (books, papers, web sites, also class material)**
  - **For web sites: include date of access**
- **Failure might be considered plagiarism**
  - **Un-ethical**
  - **Un-professional, just BAD**
  - **You will risk reporting to board of examiners and exclusion**
- **See TULIB – How to find and use scientific information http://www.library.tudelft.nl/tulib/index.htm**

Plagiarism

- So far, we found cases of plagiarism each year
- Some were severe – need to redo the project
- Multiple occurrences will make you banned from program, has happened once for student with first fraud case for this course

- Don't let it happen to you and us this year

- "Forgetting" citations: obviously forbidden
- Literal copying: obviously forbidden
- Copying of paragraph but reorganizing words: also forbidden

- "I did not know this", is not a valid excuse
  "I have not learned this before", is not a valid excuse

Report Style and Language

- 6 pages, 11 pt, A4, ‘natural’ page dimensions
- Presentation-quality figures are necessary
  - Consider resolution, contrast, legibility, SNR, …
  - Cadence-generated schematics not acceptable
- Clear equations that match surrounding text
- Always use page numbers, section numbers
- Avoid noise
  - Avoid bad grammar, bad spelling, ugly pictures, unprofessional layout, inconsistent font sizes and types, …
  - Always use a spell checker

Presentation Guidelines

- **10 minute presentation, 5 min QA**
- **Both team members should present technical details (so, 2 x 5 min)**
  Not: student A presents intro and conclusion, student B presents the rest.
  Clarify breakdown of work among team members
- **Powerpoint**
- **Typical format:**
  - **Title slide (with admin data, see report guidelines)**
  - **Introduction (context, main ideas, conceptual design, …)**
  - **Design, design steps, design choices (what, why, how, …)**
  - **Results (power, voltage, # transistors, …)**
  - **Recommendations, future work, ..**
  - **Conclusion**

Symposium

- **Tentatively week 4.3, 3 time slots**
- **Jury will read report, attend presentation, do Q&A, decide on mark**
- **University professors**

See Also

- **Class material and instructions for Introduction to Microelectronics ET4248 (essay writing, thesis writing)**
- **Also consider classes in presentation and technical writing**
- **Subsequent additions to BB and course website**