Module 2: Process

Fundamental Technology

Real men own fabs.

W.J. Saunders III, Chairman and CEO of Advanced Micro Devices Inc.

Building a new fab is like playing Russian roulette. When you build a fab, you hold the gun to your head, pull the trigger and wait three years to see if you're dead.

Unnamed IC company executive. (Integrated Circuit Design, September 1996)

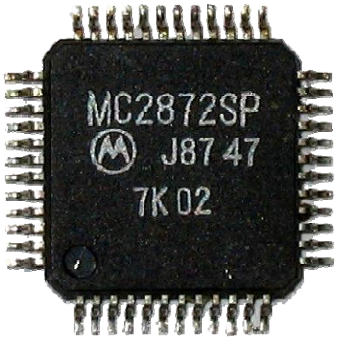
Outline

- CMOS Processing
  - Wafer Production
  - CMOS Process Outline
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Only very briefly

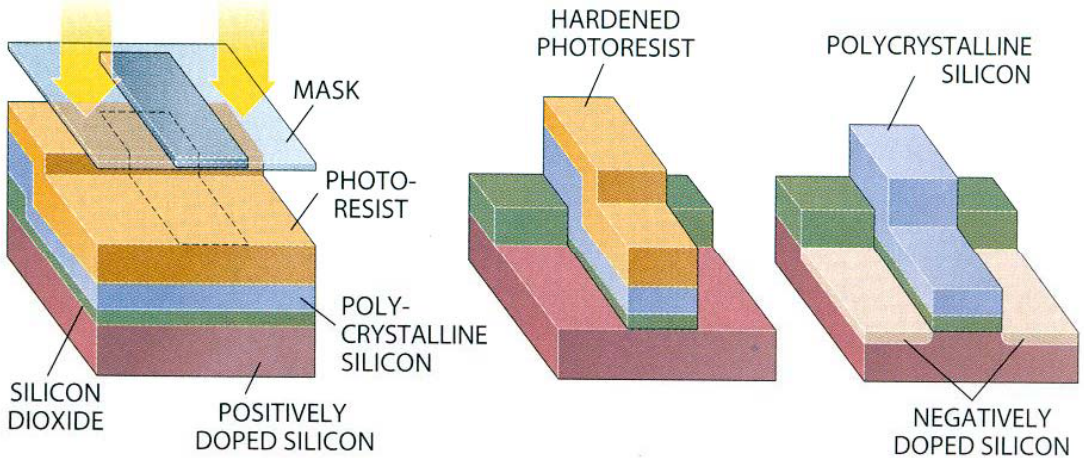
CMOS Processing

- Overview
- Photolithography
- Material Deposition & Removal
- Oxide Growth & Removal

IC Technology

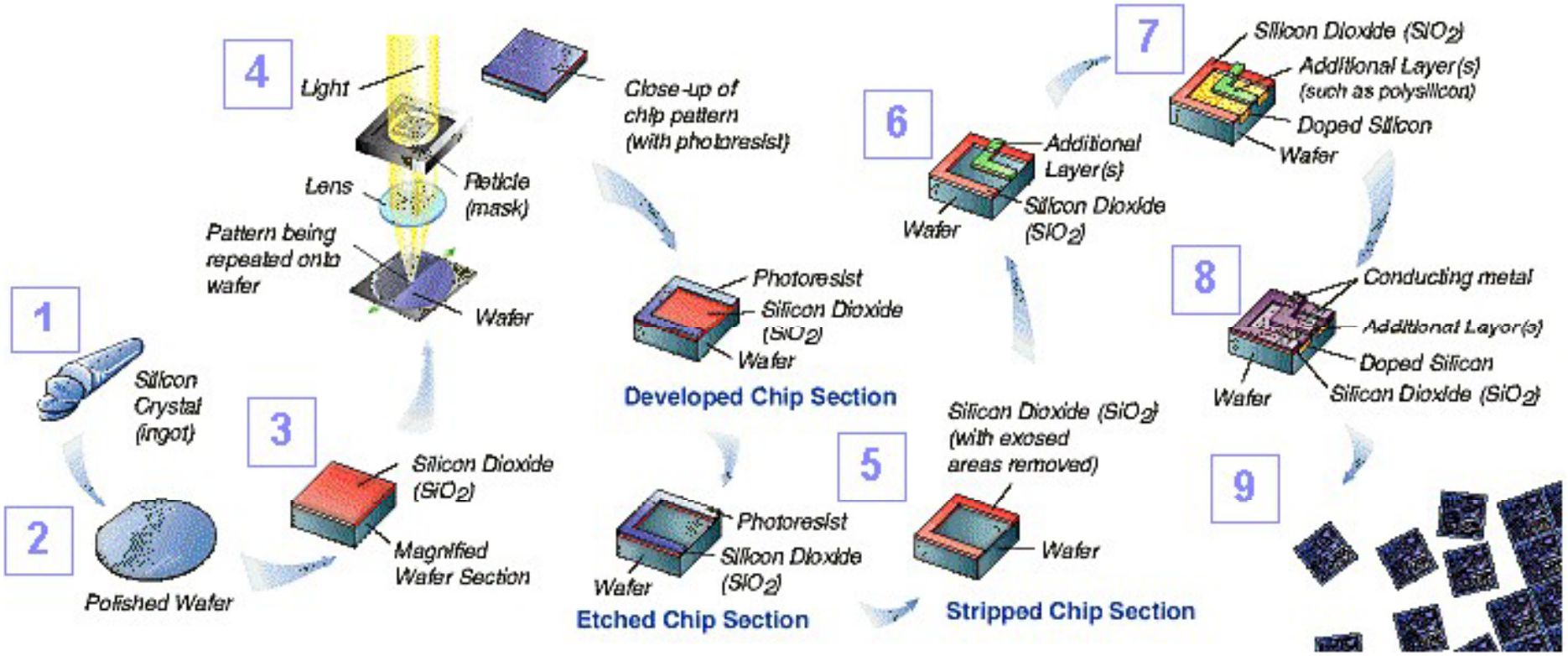


- cleaning
- deposition
- apply photoresist
- exposure
- development
- etching
- remove resist



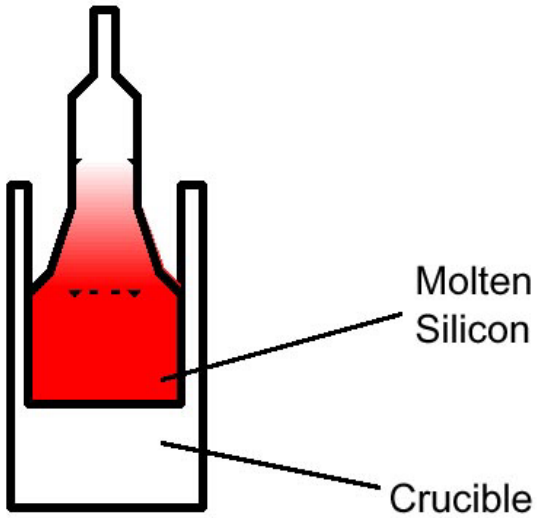
Multiple cycles, 100's STEPS in total

Another Overview of Semiconductor Processing

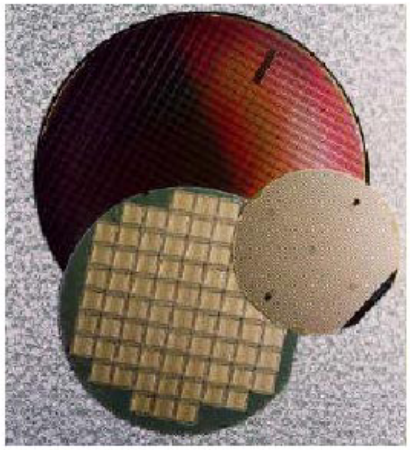


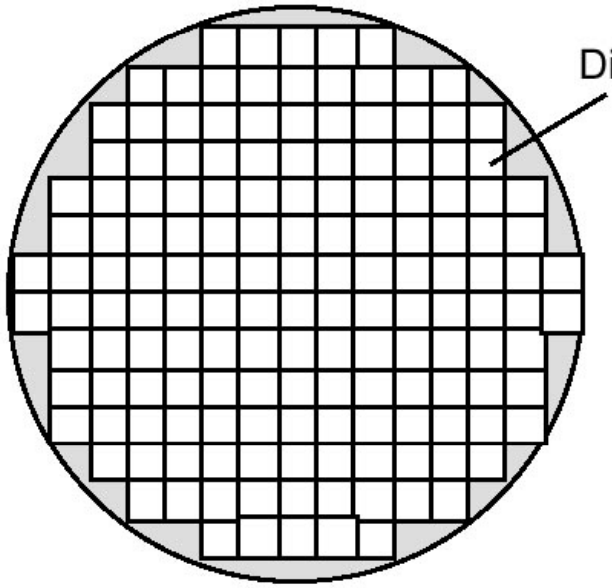
Wafer Processing – Czochralski Method

- **Start with crucible of molten silicon (≈1425ºC)**
- **Insert crystal seed in melt**
- **Slowly rotate/raise seed to form single crystal boule**
- **After cooling, slice boule into wafers & polish**



Wafer Structure

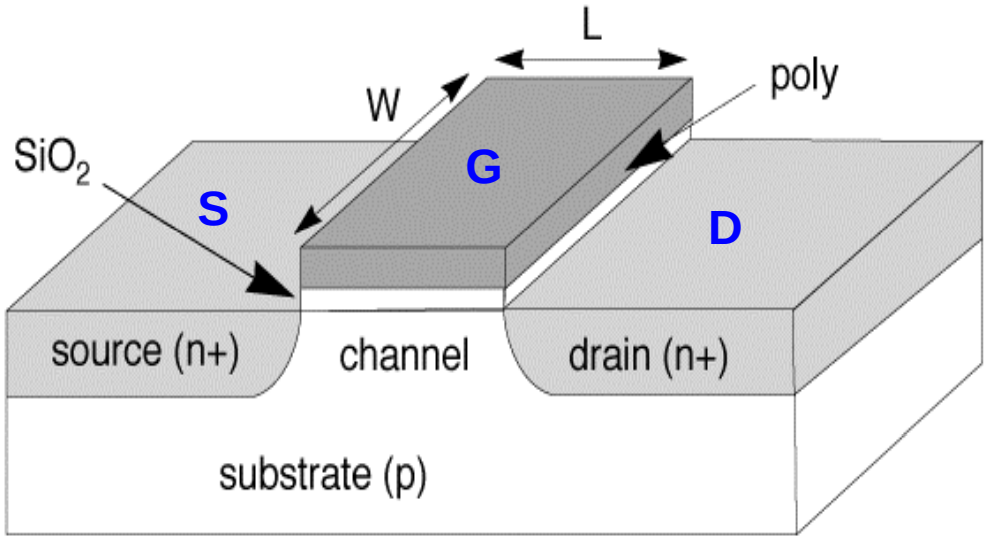


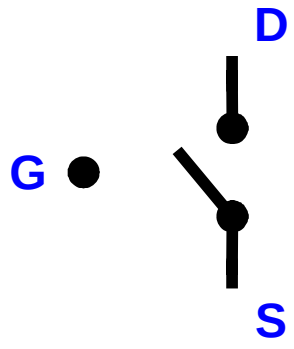


300 mm wafer (sematech)

CMOS Process Outline

MOS Transistor



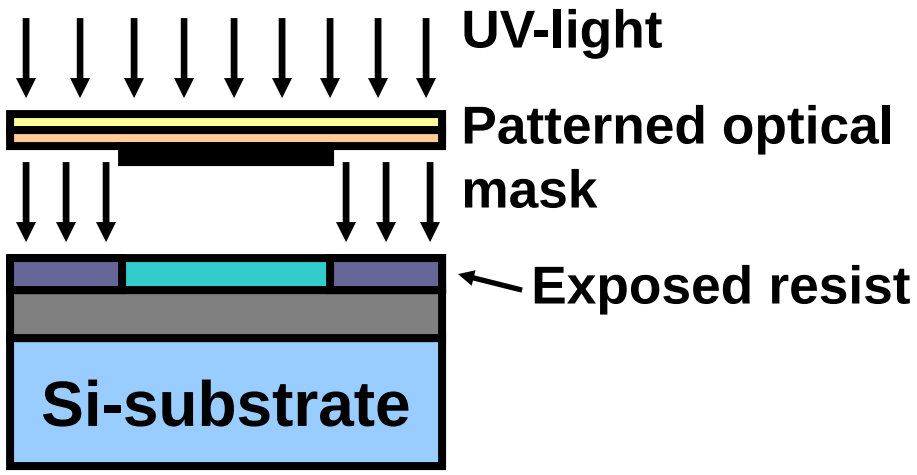


Position of switch depends on gate to source voltage

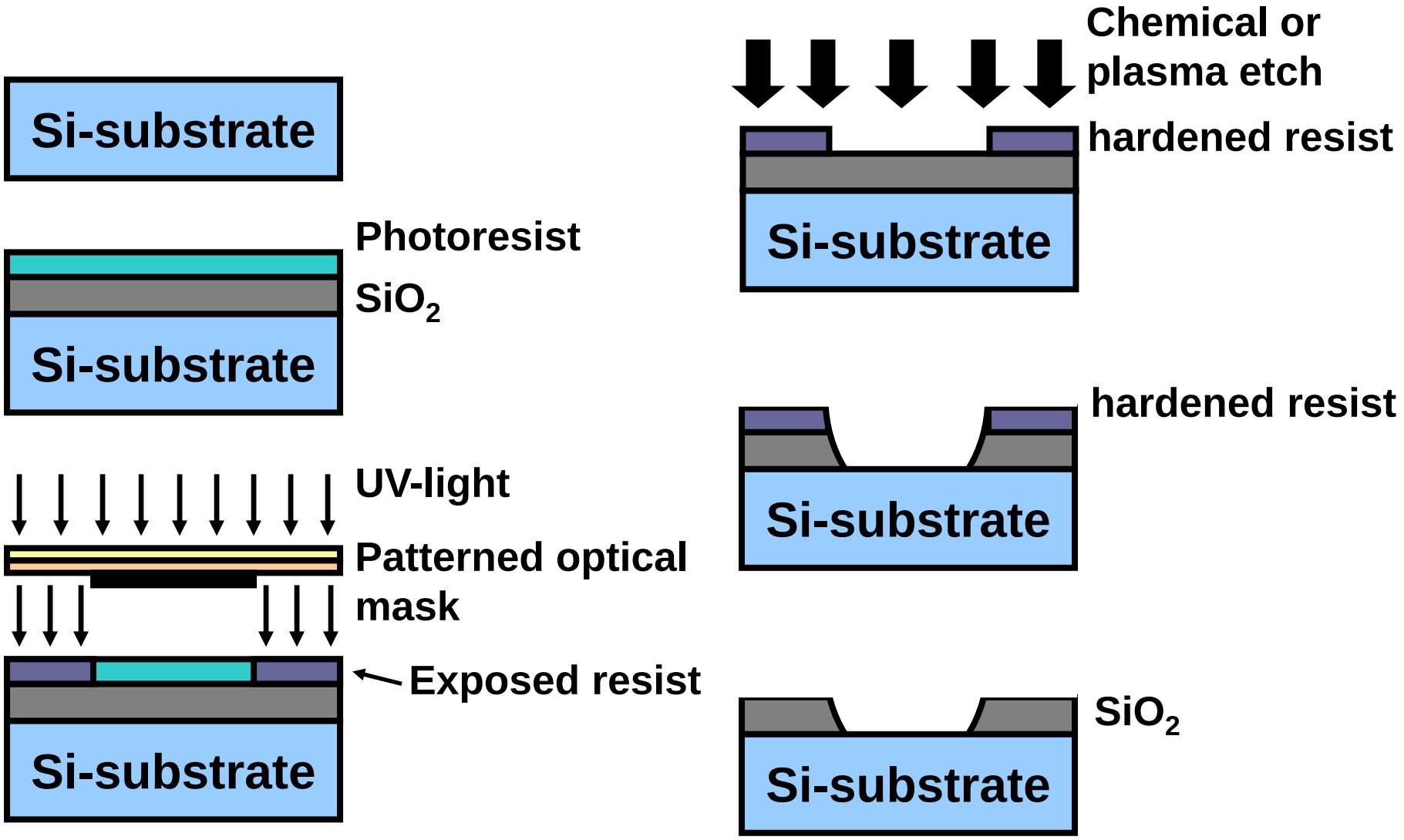
V_{GS}	NMOS	PMOS
hi	closed	open
lo	open	closed

How Patterns on a Chip are Created

- **Basic Principle: Photolithography**
  - **Like projecting an image through a photographic negative (or positive)**
- **Coat wafer with Photoresist**
- **Shine UV light through glass mask**
- **Develop: dunk in acid to remove exposed areas ("pos.") or unexposed areas ("neg.")**



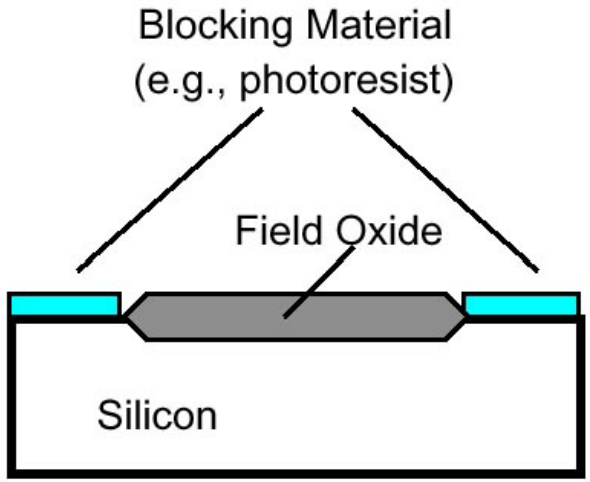
Example: Etching Step, opening of SIO_2



Etching is for removal of material, similar masking principles for deposition (adding of material)

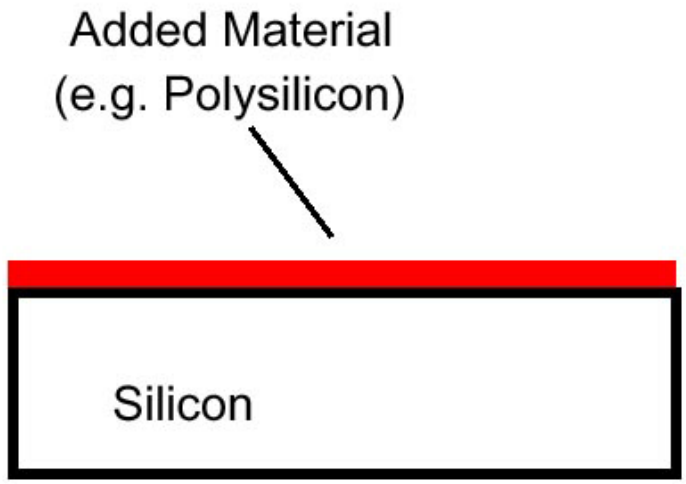
Oxidation

- **SiO_2 formed by oxidation**
  - **Wet oxidation: heat with water (900ºC - 1200 ºC)**
  - **Dry oxidation:heat with pure oxygen (1200 ºC)**
- **Oxide occupies more volume**
- **Alternative: deposition**



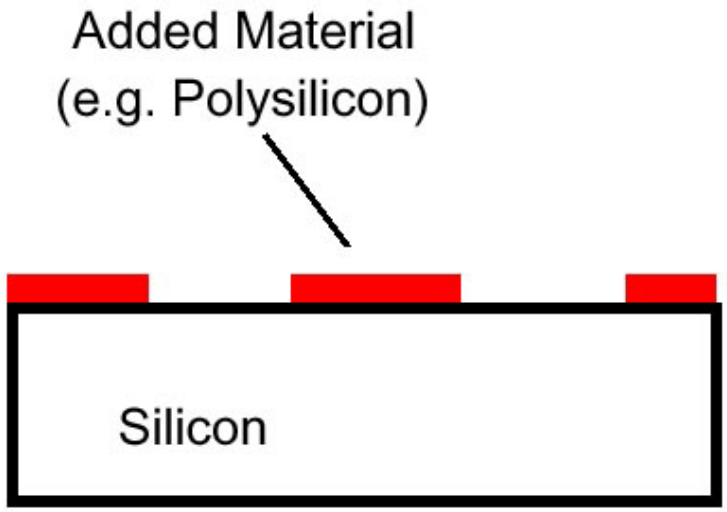
Adding Materials

- **Add materials on top of silicon**
  - **Polysilicon**
  - **Metal**
  - **SiO_2**
- **Methods**
  - **Vapor deposition**
  - **Sputtering (Metal ions)**



Patterning Added Materials

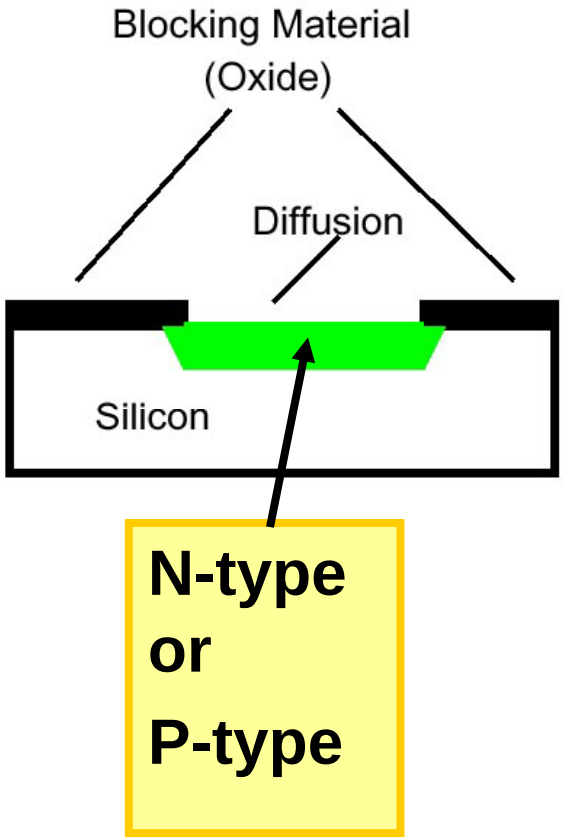
- **Add material to wafer**
- **Coat with photoresist**
- **Selectively remove photo resist (PR), after exposure through mask**
- **Remove unprotected (by PR) material**
- **Remove remaining PR**



Diffusion

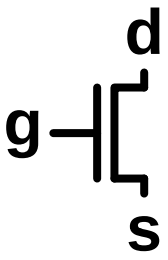
- Modify electrical properties of Si:
  - N-type (extra electrons)
  - or p-type

    (fewer electrons ⇔ extra holes)
- Introduce dopant via epitaxy or ion implant e.g. Arsenic (N), Boron (P)
- Allow dopants to diffuse
- Block diffusion in selective areas using oxide or PR (photo-resist)
- Diffusion spreads both vertically, horizontally



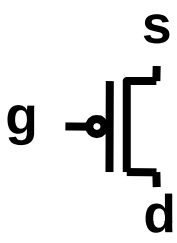
CMOS – *Complementary* Metal Oxide Semiconductor Technology

2 Distinct Transistor Types



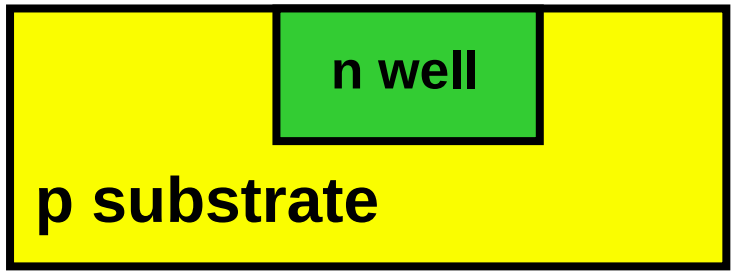
n-type

- **“on” when V_g is high**
- **With n-type s/d**
- **Electrons (n) as carrier**
- **Built in p-type Si**



p-type

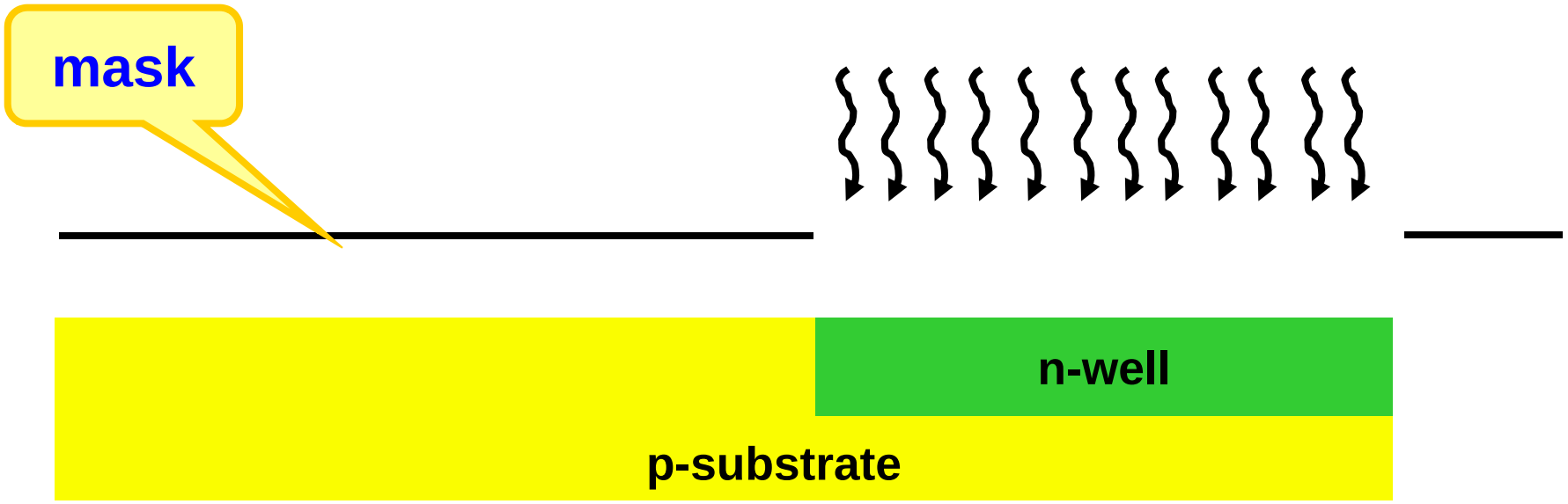
- **“on” when V_g is low**
- **With p-type s/d**
- **Holes (p) as carrier**
- **Built in n-type Si**



n-well (for PMOS) in p-type substrate (for NMOS)

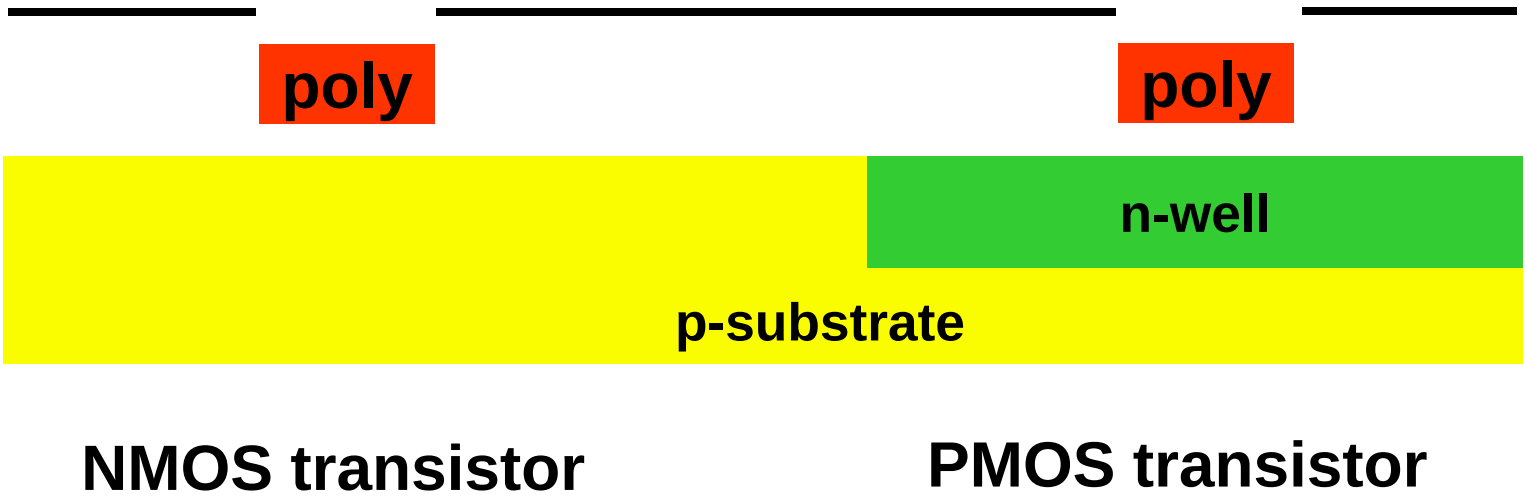
Outline of Process Flow

First place n-well to provide properly-doped substrate for n-type, p-type transistors :



Outline of Process Flow, cont'd

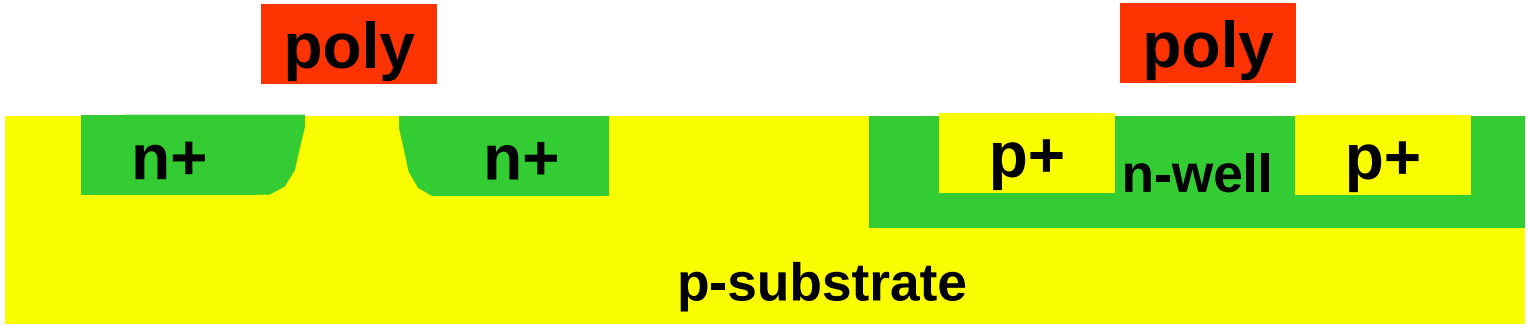
Pattern gate next, to later act as a mask for source and drain diffusions:



Outline of Process Flow, cont'd

Add s/d diffusions, performing self-masking by poly gate:

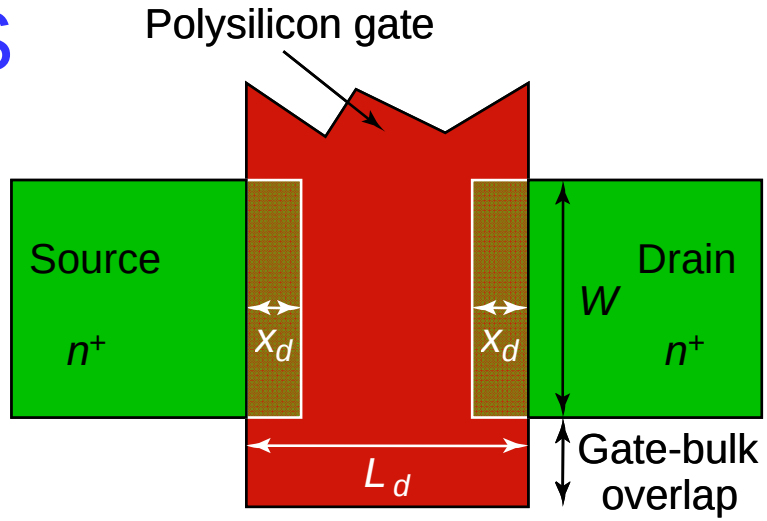
Poly also works as a mask, ensuring good alignment of s/d to gate



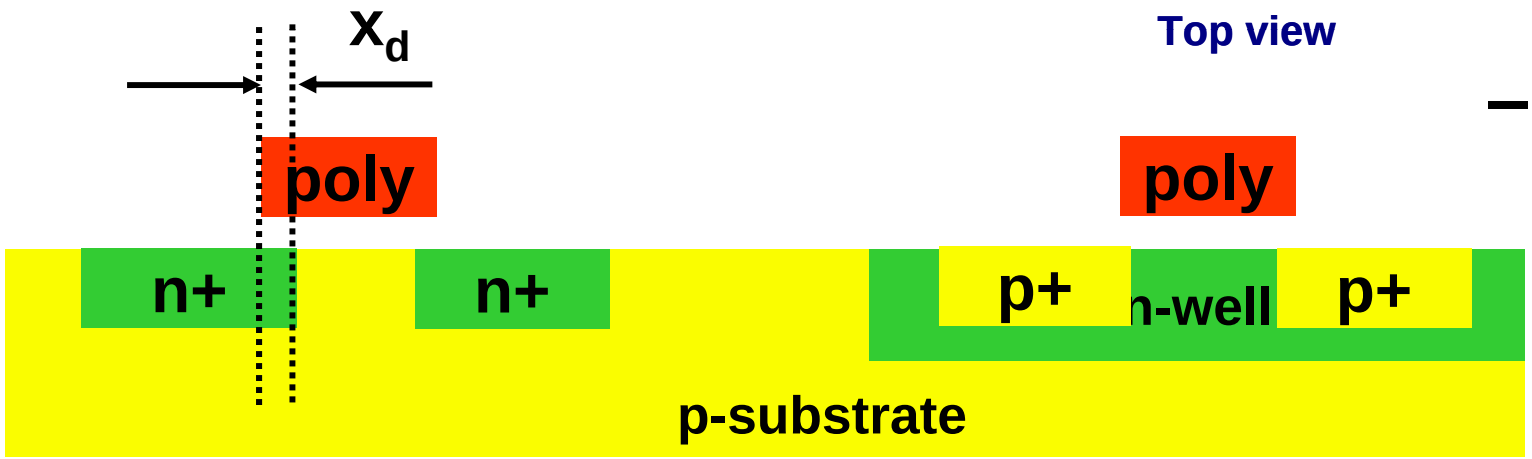
NMOS transistor **PMOS transistor**

TPS

- What is the cause of x_d?
- Why do we want it?



Top view

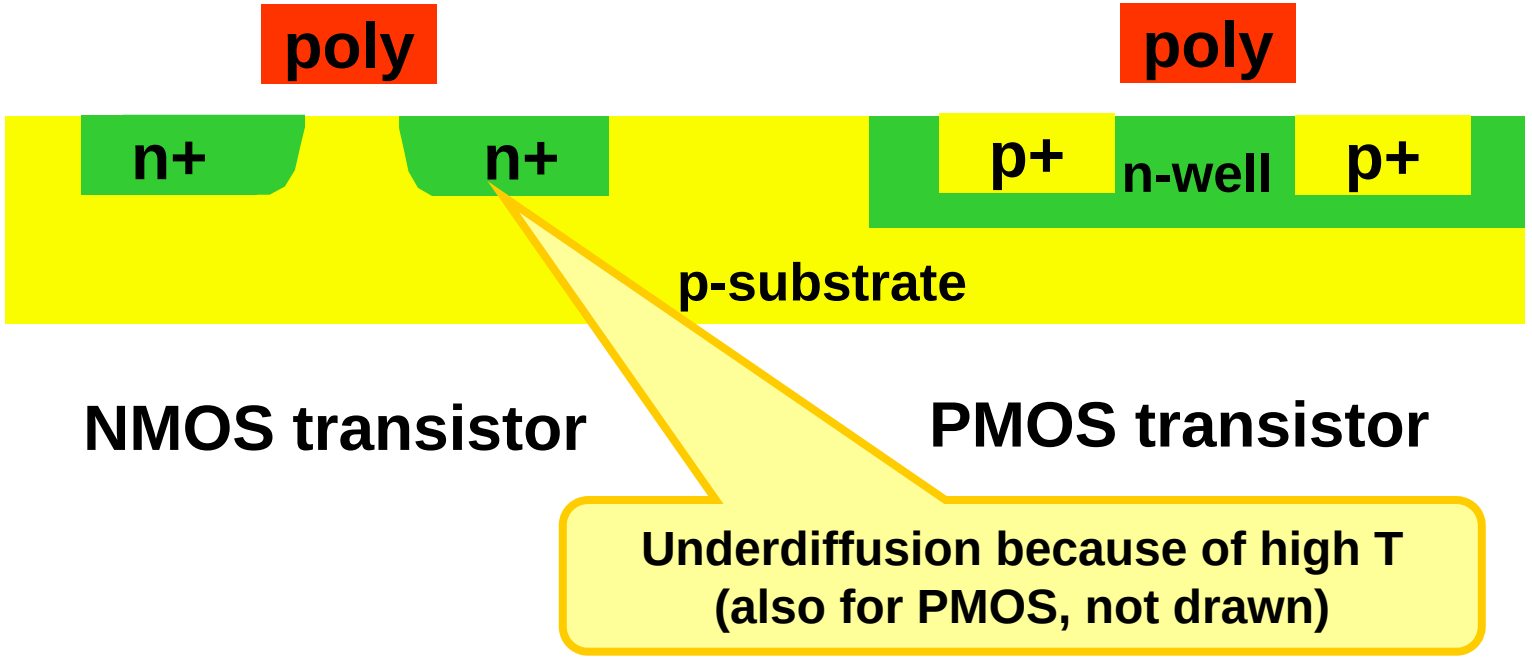


NMOS transistor

PMOS transistor

Outline of Process Flow, cont'd

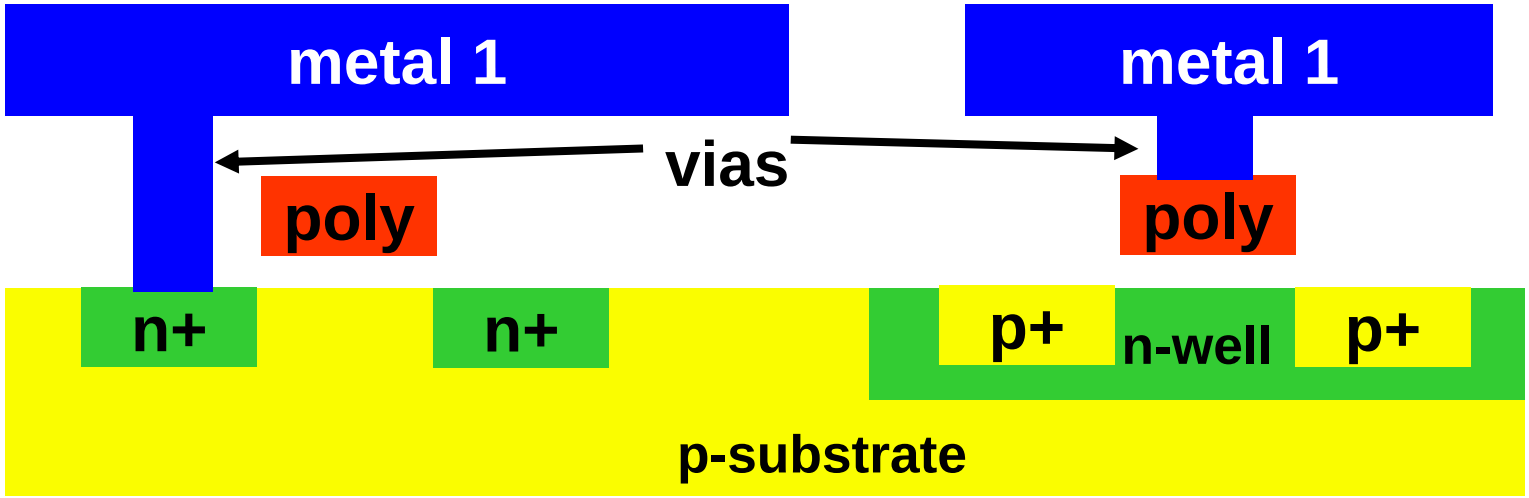
Add s/d diffusions, performing self-masking by poly gate:



Outline of Process Flow, cont'd

Start adding metal layers:

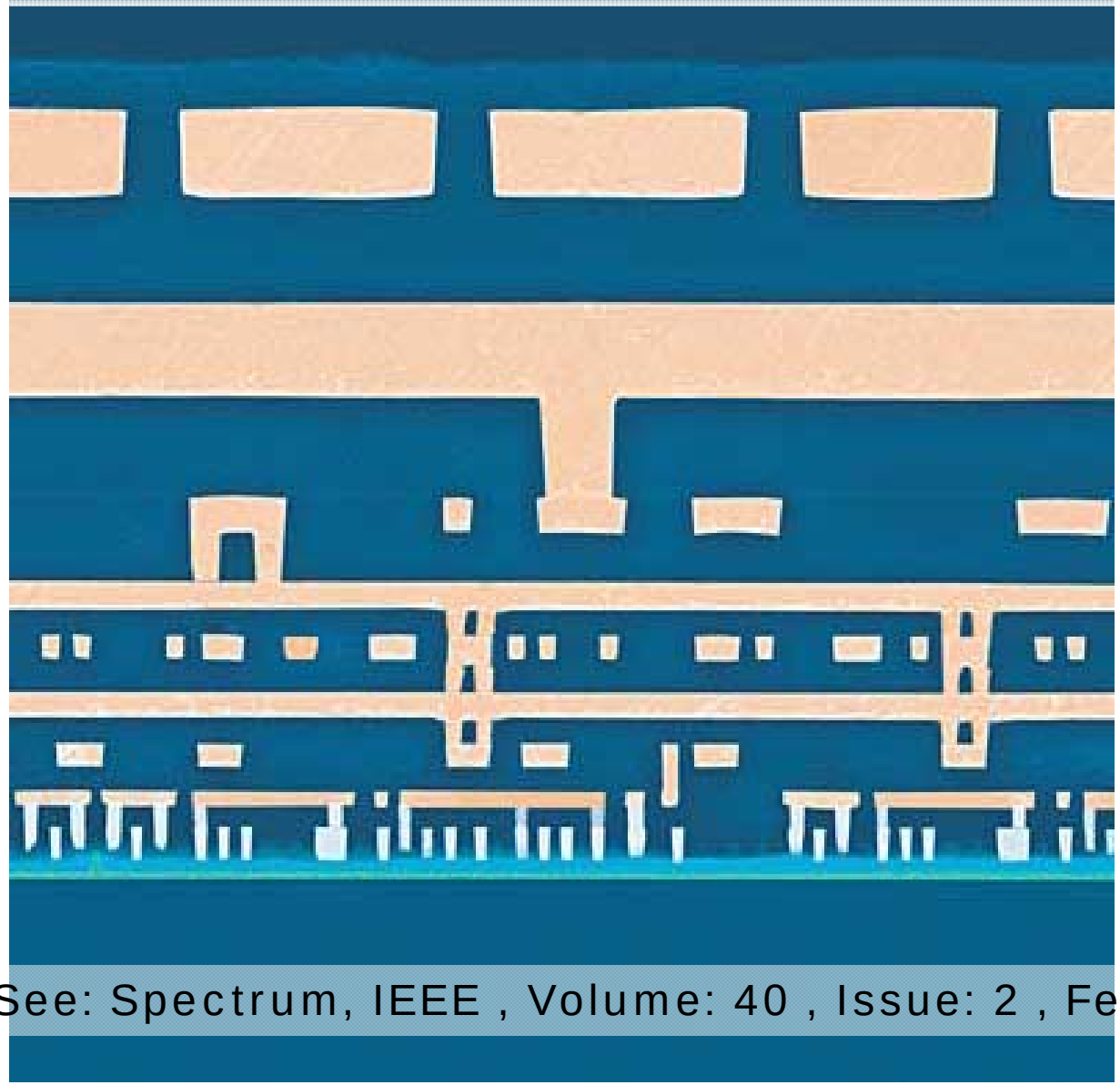
Via: contact hole between metal layers



NMOS transistor **PMOS transistor**

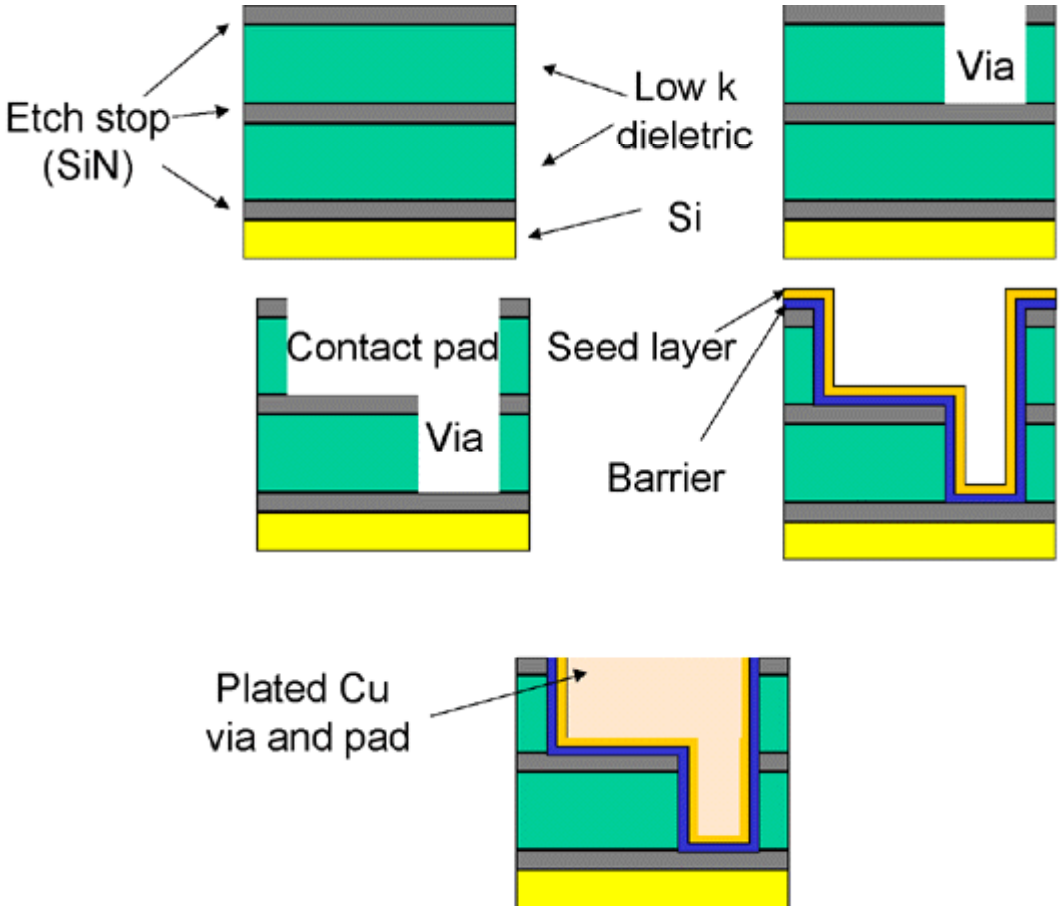
Similar for subsequent metal layers

Cross-section of IBM CU process



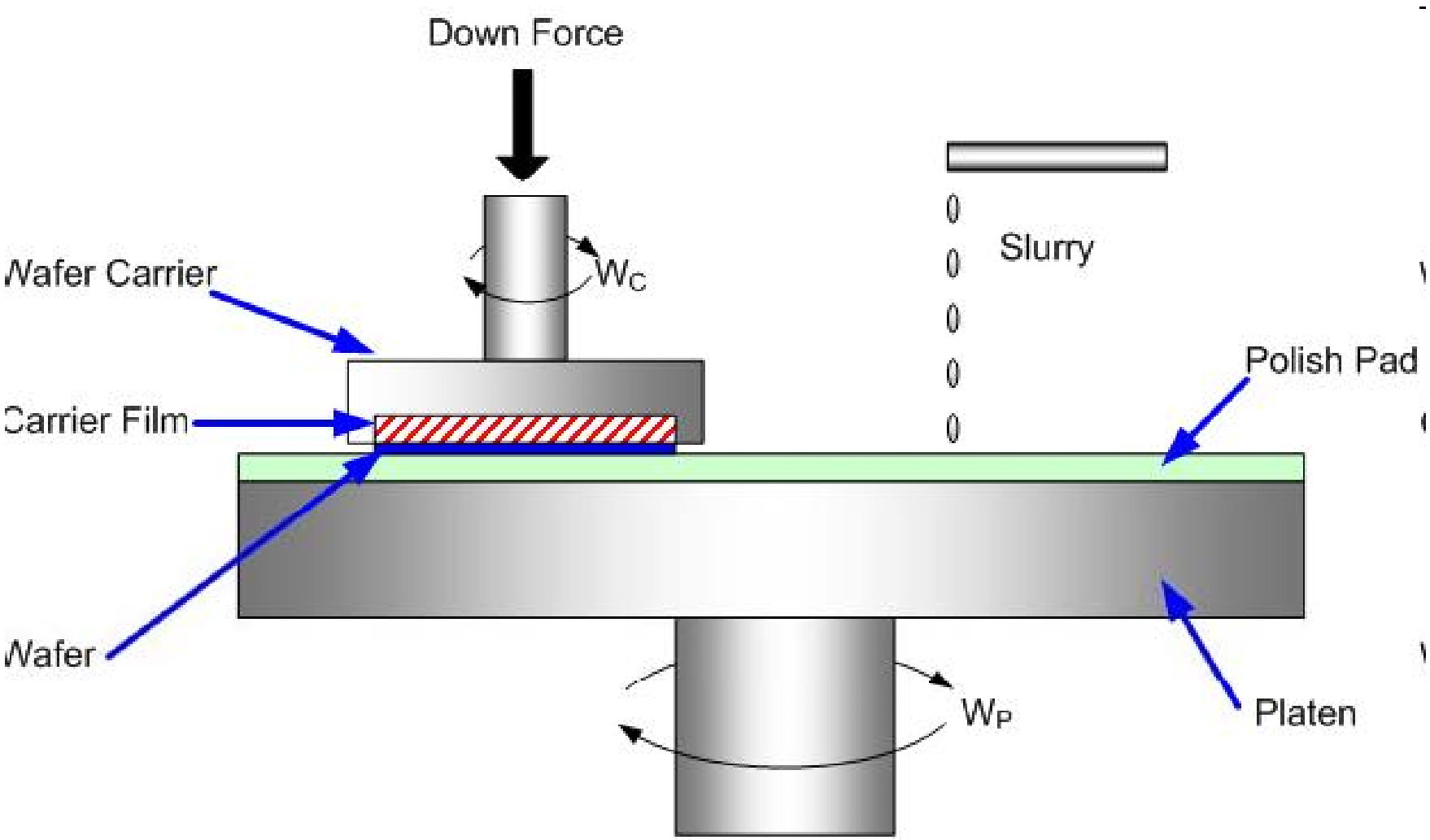
See: Spectrum, IEEE , Volume: 40 , Issue: 2 , Feb. 2003

IBM Dual Damascene Metal Depostion



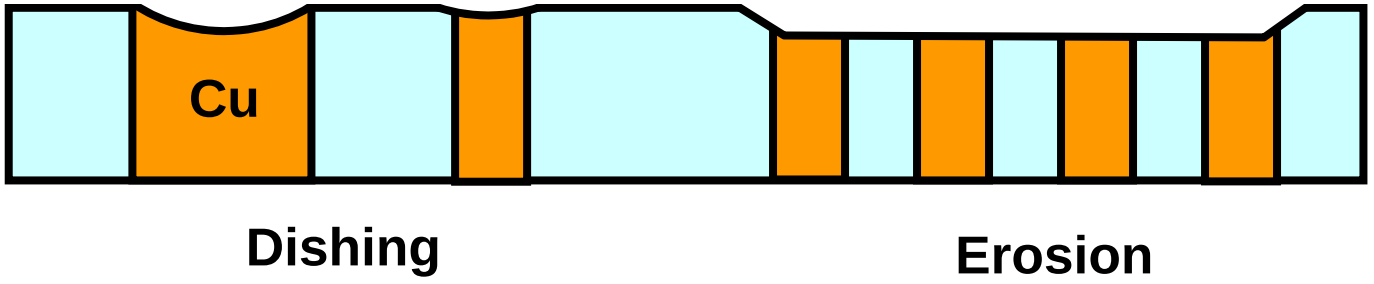
[http://www.tms.org/pubs/journals/JOM/9903/Frear-9903.fig.5.lg.gif]

CMP – Chemical Mechanical Polishing

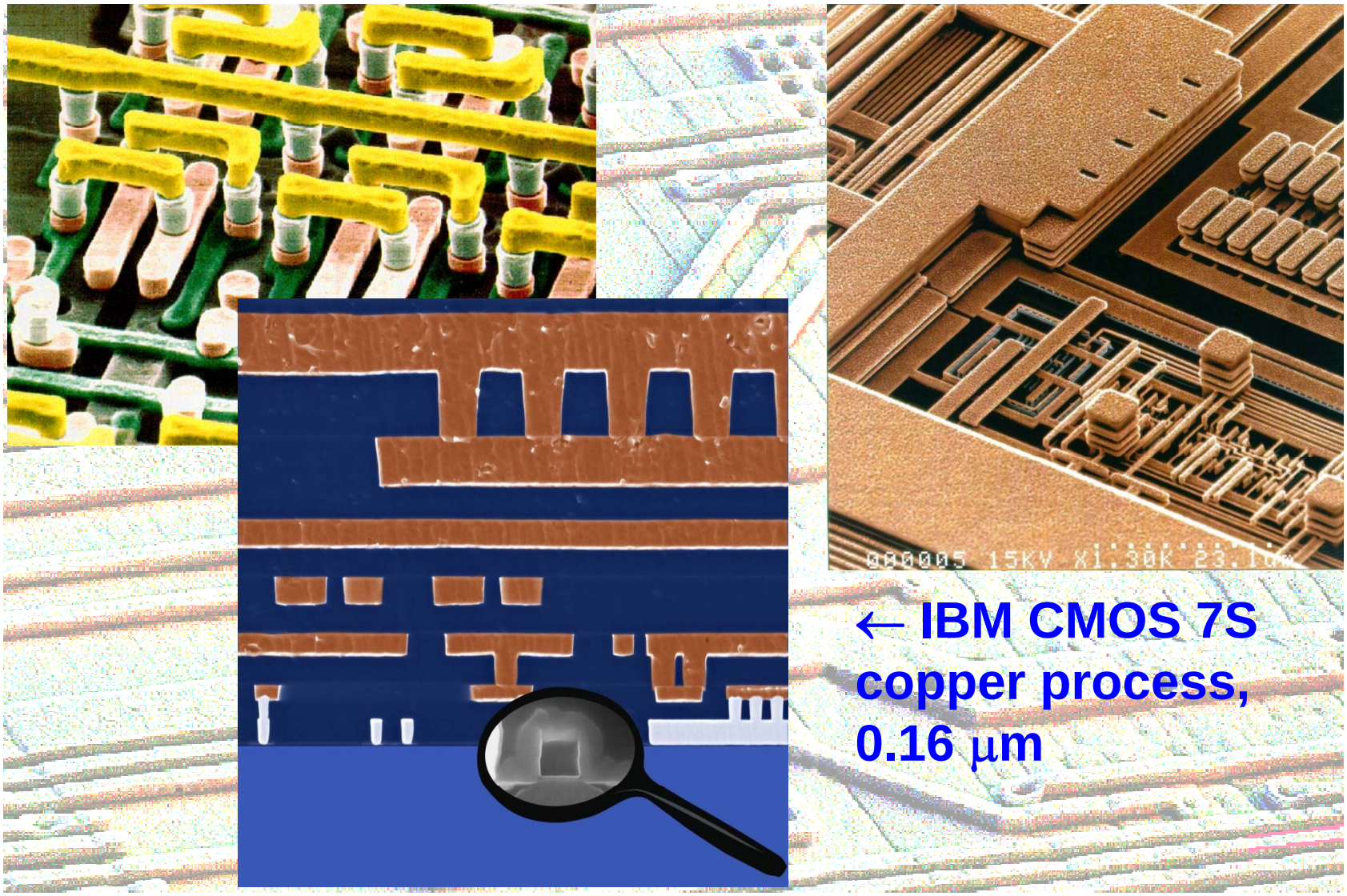


Metal CMP Variability Effects

- **Systematic, layout-process interaction**
- **Die-level**
- **Effect can be modeled with ‘local layout density’ concept**
- **(Effective) metal height**
- **Density function from selectivity of chemical polishing combined with mechanical/chemical ‘protection’ from dielectric**
  - **Wide metal sensitive to thinning**
  - **Narrow dielectric sensitive to erosion**



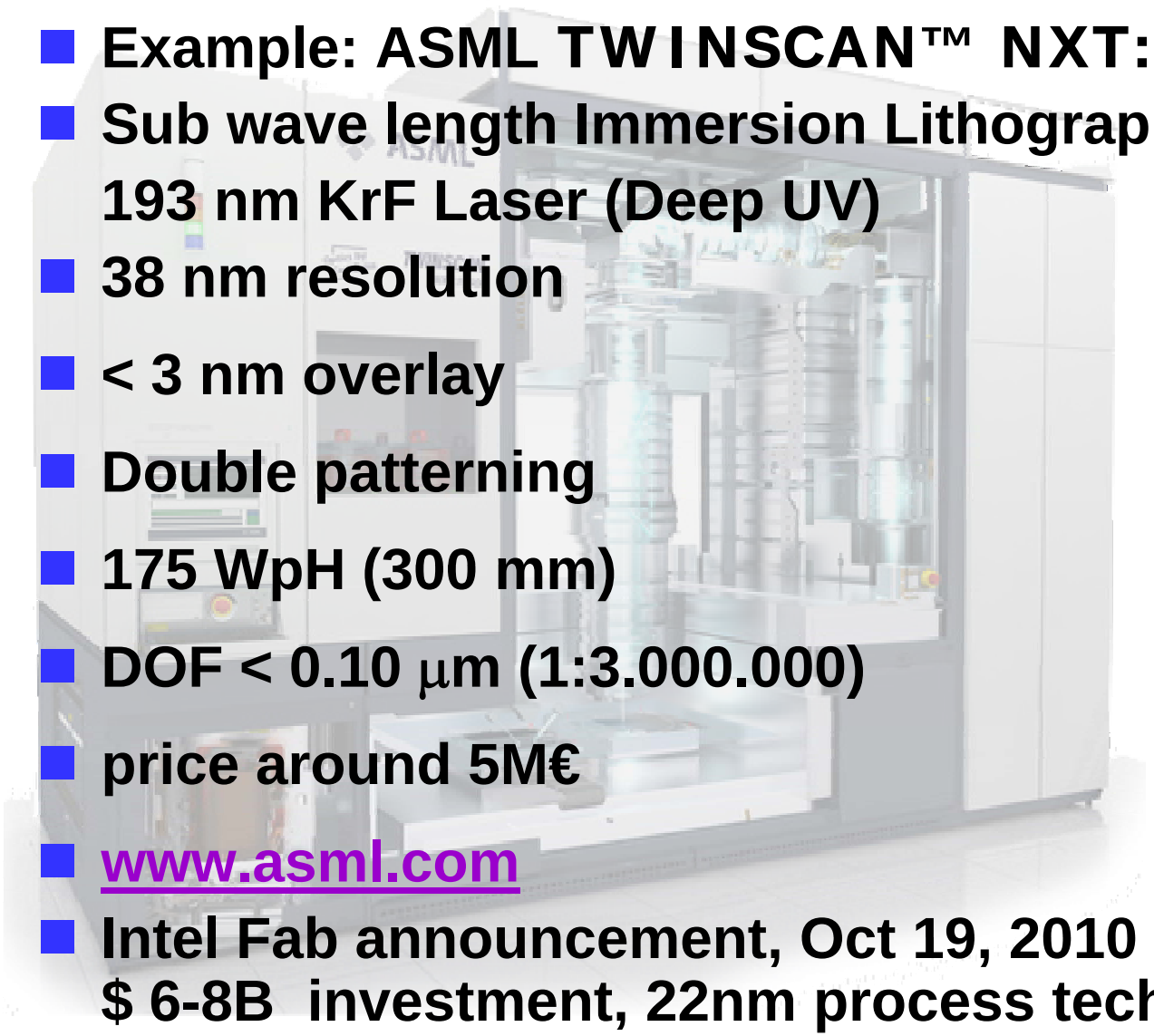
Interconnect Examples (motorola, ibm)



IC Recipe Precisely Fixed

- **Process conditions (temperature, time, concentration, ...) very critical**
- **Many strong compatibility issues of materials and processes**
- **Very expensive and difficult to tune**
- **Very expensive equipment and facilities**
- **Need Billions of turnover for break-even**

Complex Lithographic Process



- **Example: ASML TWINSCAN™ NXT:1950i**
- **Sub wave length Immersion Lithography**
  193 nm KrF Laser (Deep UV)
- **38 nm resolution**
- **< 3 nm overlay**
- **Double patterning**
- **175 WpH (300 mm)**
- **DOF < 0.10 μm (1:3.000.000)**
- **price around 5M€**
- **www.asml.com**
- **Intel Fab announcement, Oct 19, 2010**
  $ 6-8B investment, 22nm process technology

ASML EUV Tool Development

Compare Stepper Wafer Size and Resolution to NL scale

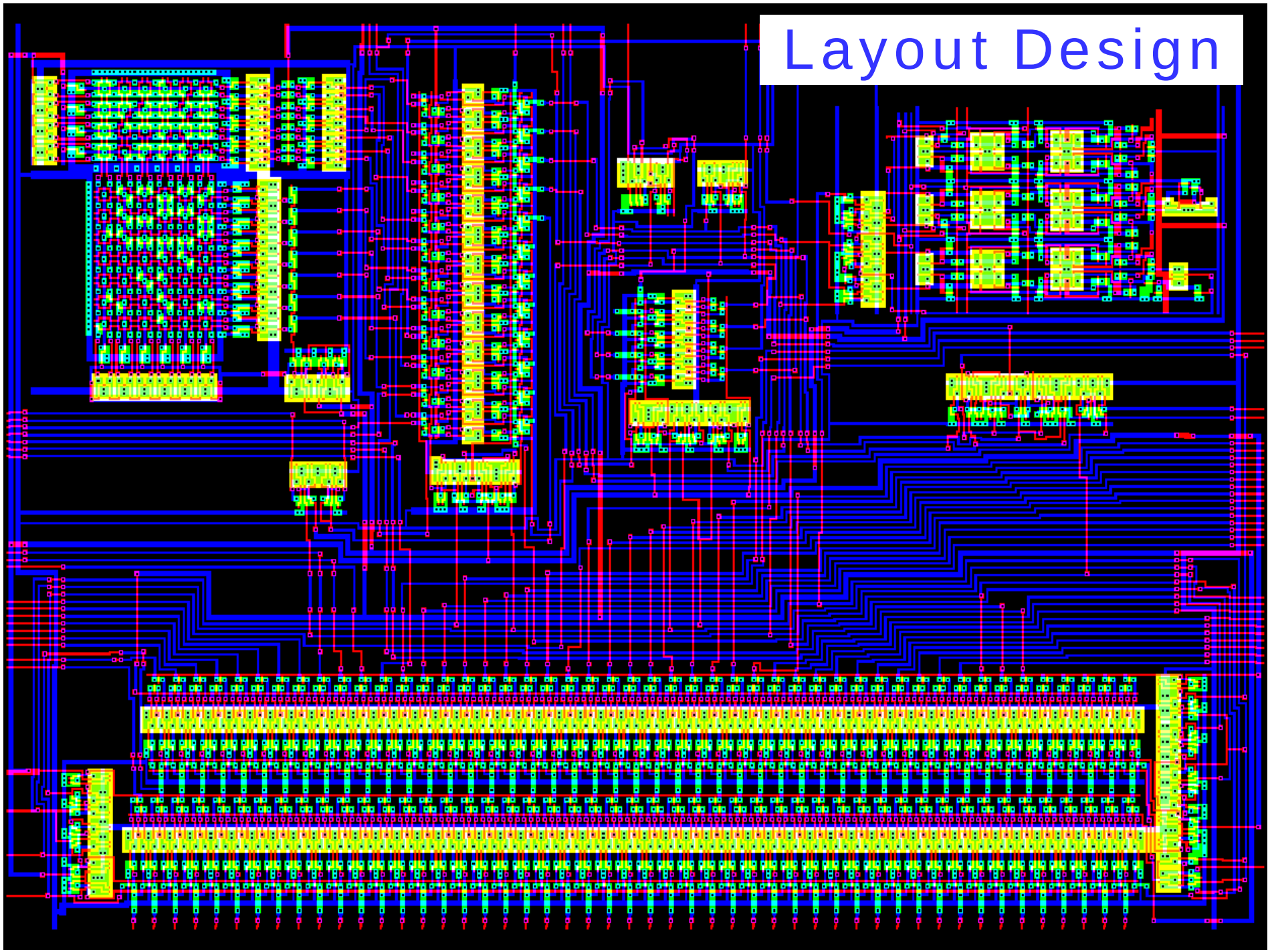
- **Wafer size: ∅ 300 mm**
- **Resolution: 38nm**
- **Netherlands: 40.000 km^2 ~ ∅ 225 km**

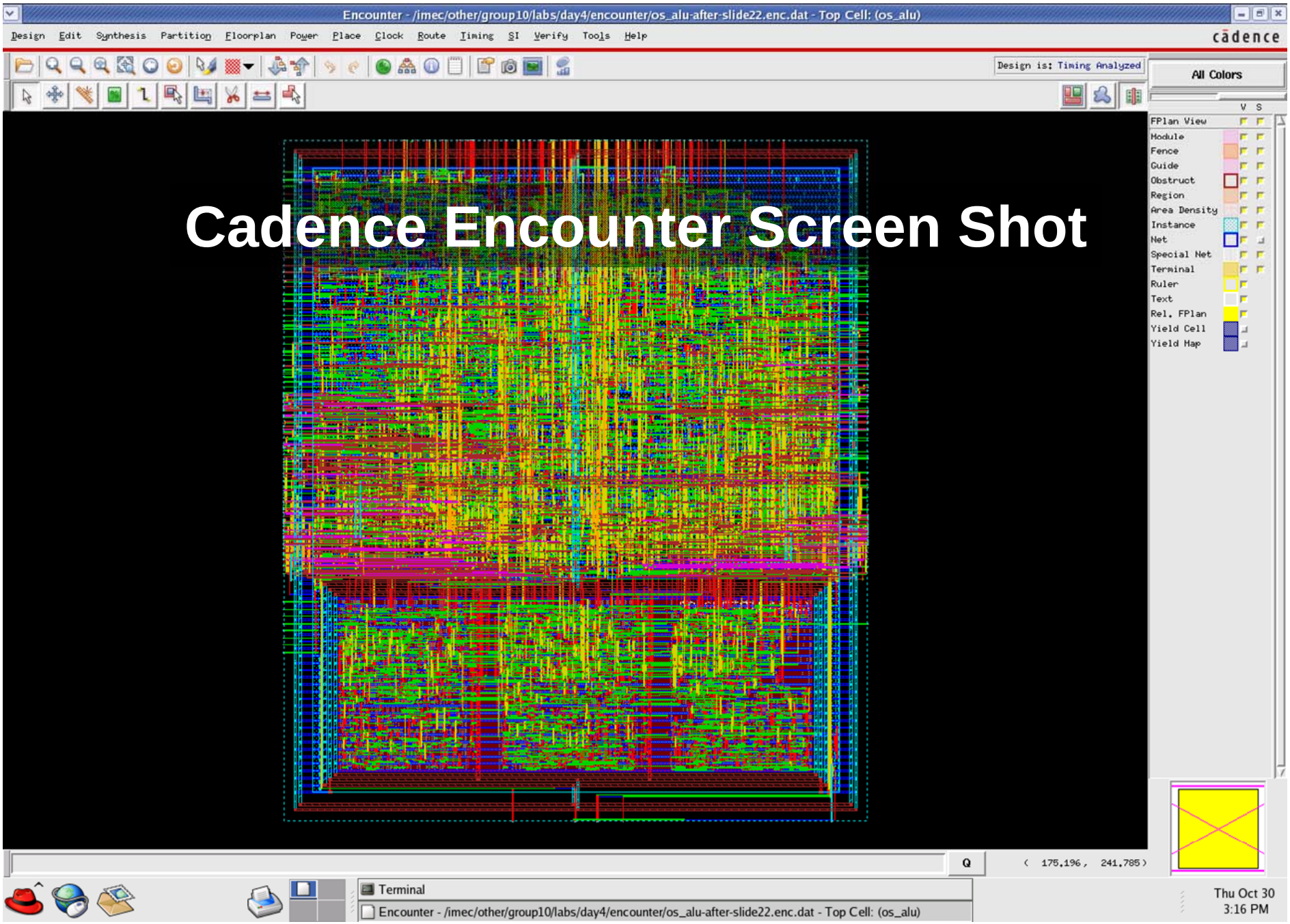
300 mm	**1**	**22 nm**
225 km	**750x10^3**	**1.7 cm**

A ‘magnified’ waferstepper could ‘print’ the Netherlands with a resolution of 1.7 cm in 20 sec.

About equal to a 185 terabit camera ~ 10 Million 20 megapixel cameras (B/W)

Layout Design

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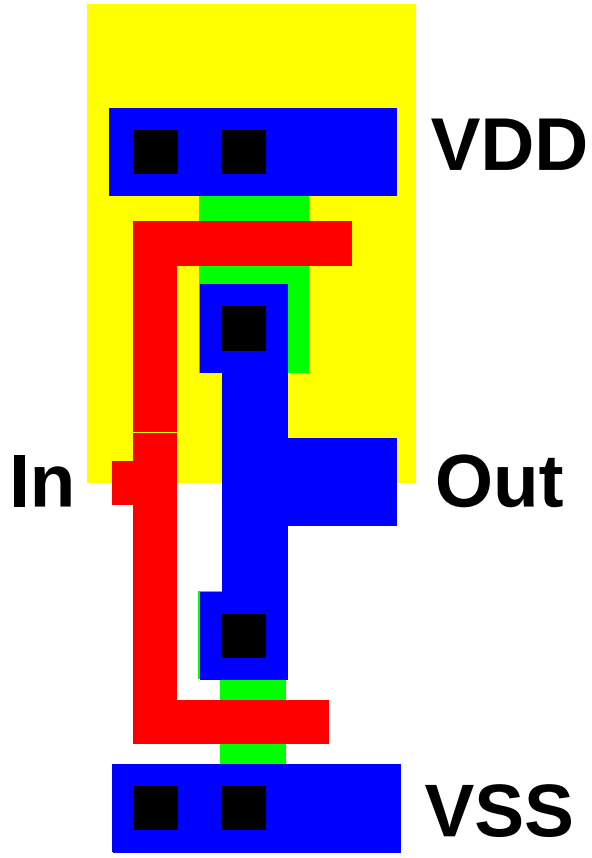
Layout Design

Layout Design Concepts

- **Layer map**
- **Layout examples**
- **Stick diagrams**



You should be able to understand such a drawing as well as simpler drawings called ‘stick diagram’

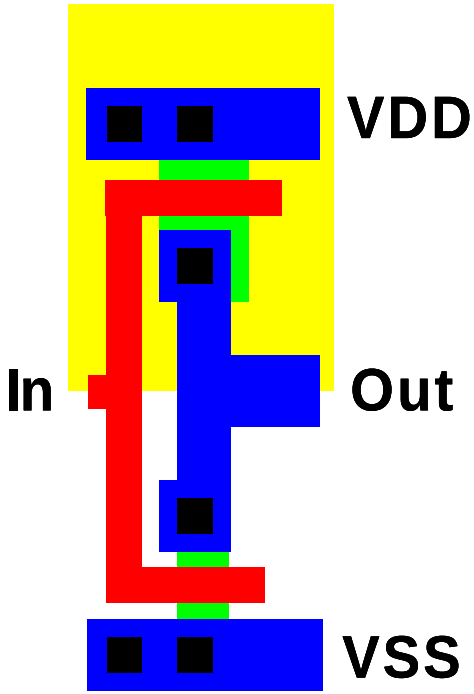
Layout Design

- Layout is design of fabrication masks
- Each mask is drawn in different color
- Layout is not a free-form drawing

  Most often: Manhattan Layout (rectangular)

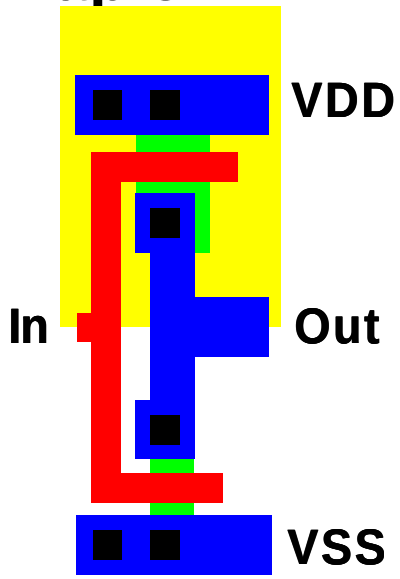
  Sometimes 45-degree angles

  Curved geometry only for special applications
- Layout should obey Design Rules



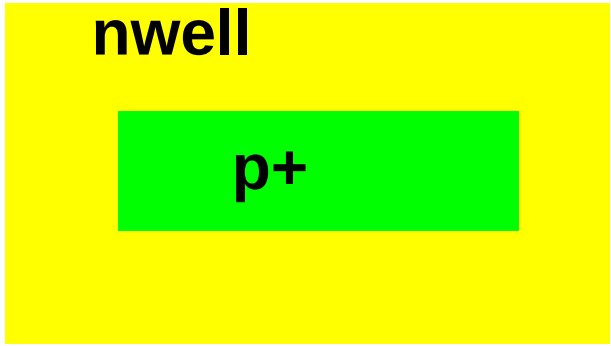
Layer Map

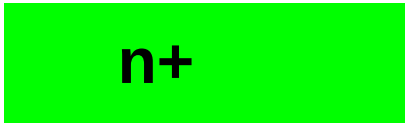
- **Layers are assigned colors and/or patterns, not always 1 to 1**
- **Is a matter of convention**
- **Site-dependent, process dependent, tool dependent**
- **Be prepared to reverse-engineer layer map of unknown layouts**



Polarity of Active Area

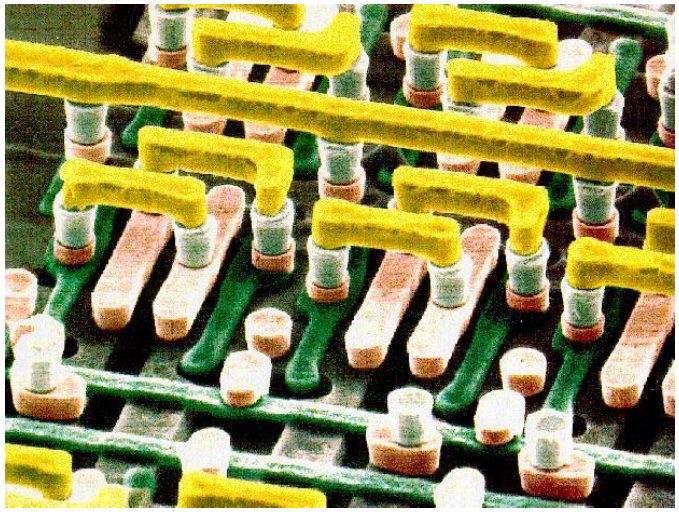
- **Active layer or active area is the source/drain implant layer (area). Usually abbreviated as 'active' only.**
- **Normally, a so-called select mask determines polarity of active**
- **See color plate 5**
- **Many simplified drawings only show subset of the masks**
- **Rest should be clear from context**

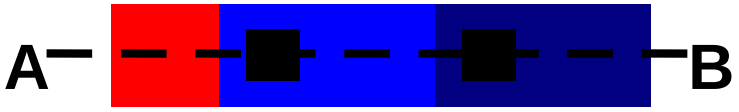




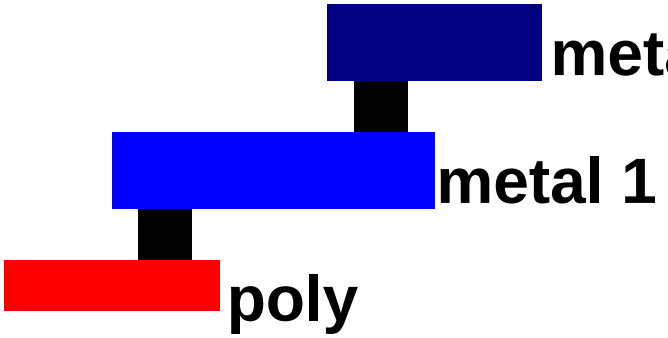
active

Contact Holes and Vias





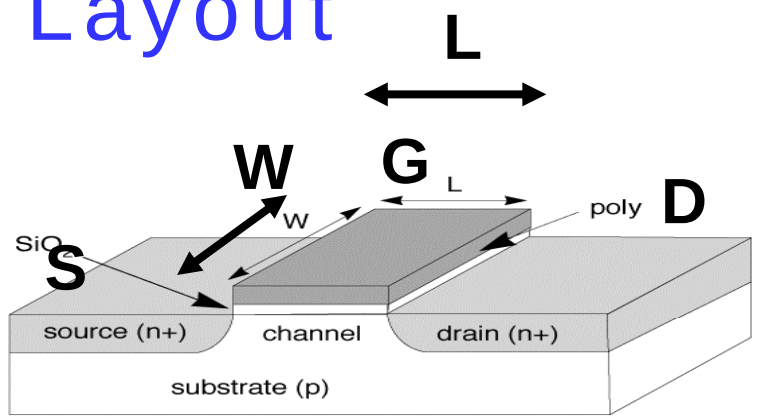
Layout (top view)



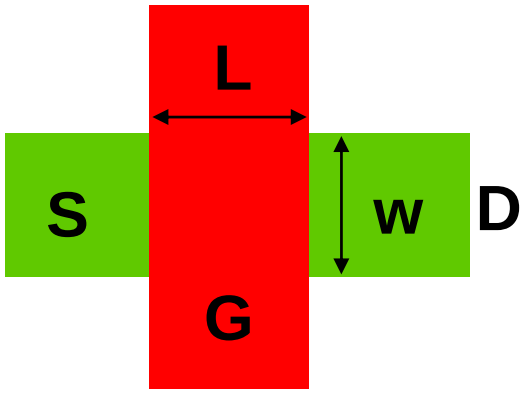
Cross-section along A-B

Transistor Layout

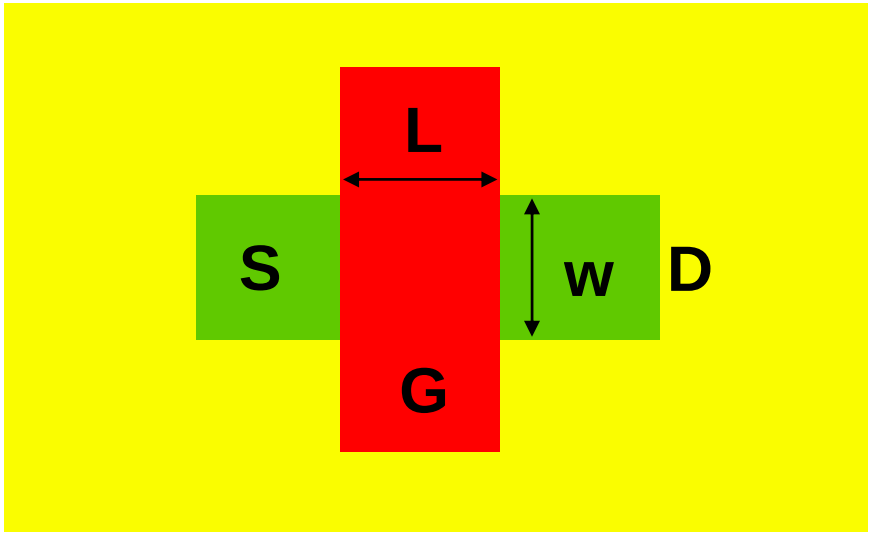
n-well (p-sub)



n-type



p-type



Simplified CMOS Layer Map

- **Compare to / instead of colorplate 1.**

yellow		**nwell – place for P-transistors**
pink		**select – invert polarity of active**
green		**active – source and drain regions**
red		**polysilicon – gate material**
blue		**metal 1 – first interconnect metal**
dark blue		**metal 2 – second interconnect metal**
magenta		**metal 3 – third interconnect metal**
black		**contact, via – hole in interlayer oxide**

- **Note: active = active area = diff = diffusion, well ≈ tub**

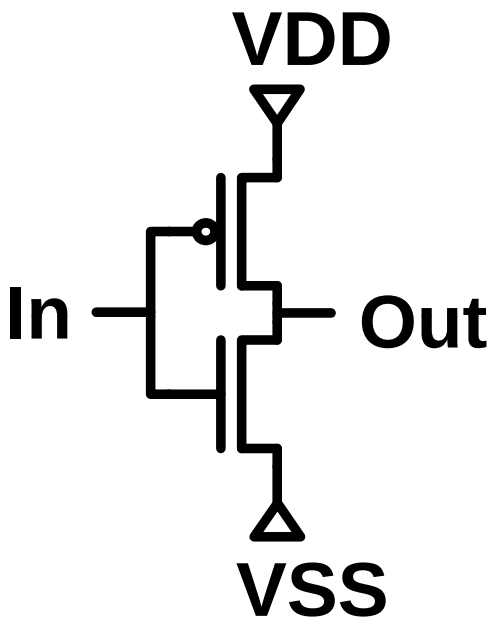
Further Simplified CMOS Layer Map

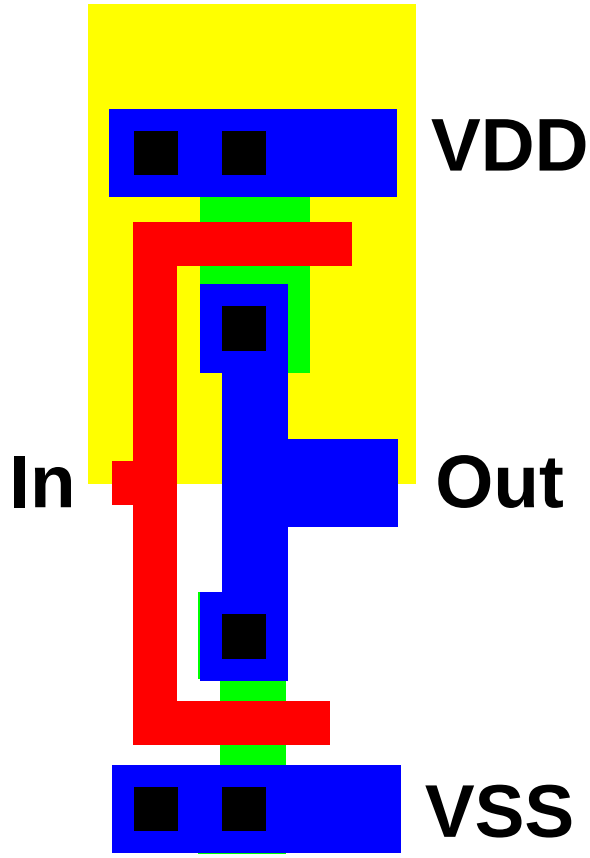
- **Compare to / instead of colorplate 1.**

yellow		**nwell – place for P-transistors**
green		**active – source and drain regions**
red		**polysilicon – gate material**
		**metal 1 – first interconnect metal**
black		**contact, via – hole in interlayer oxide**

- **Or equivalent B/W patterns**

Invertor Layout



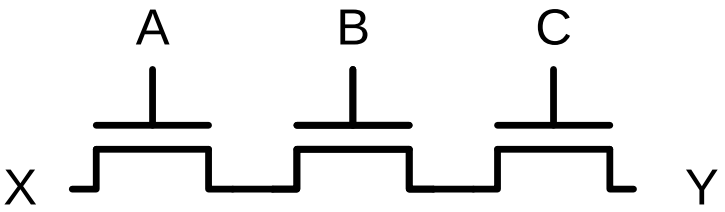


Assignment 2

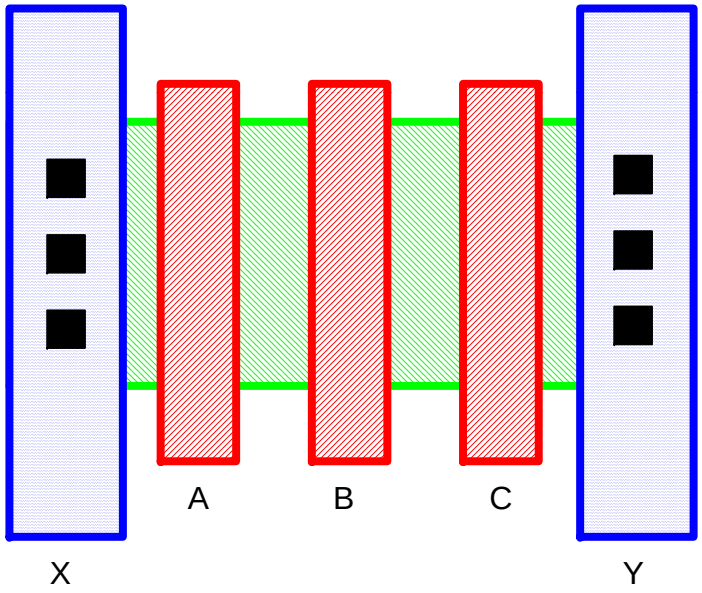
Main difficulty: you need to guess/extrapolate covered portions of the layout (e.g. green under blue)

Be able to draw such layouts (but more complex) (layout assignment) and reverse engineer (decode) them

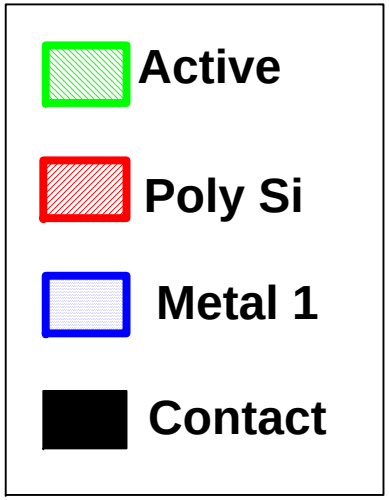
From Schematic to Layout



Transistor schematic



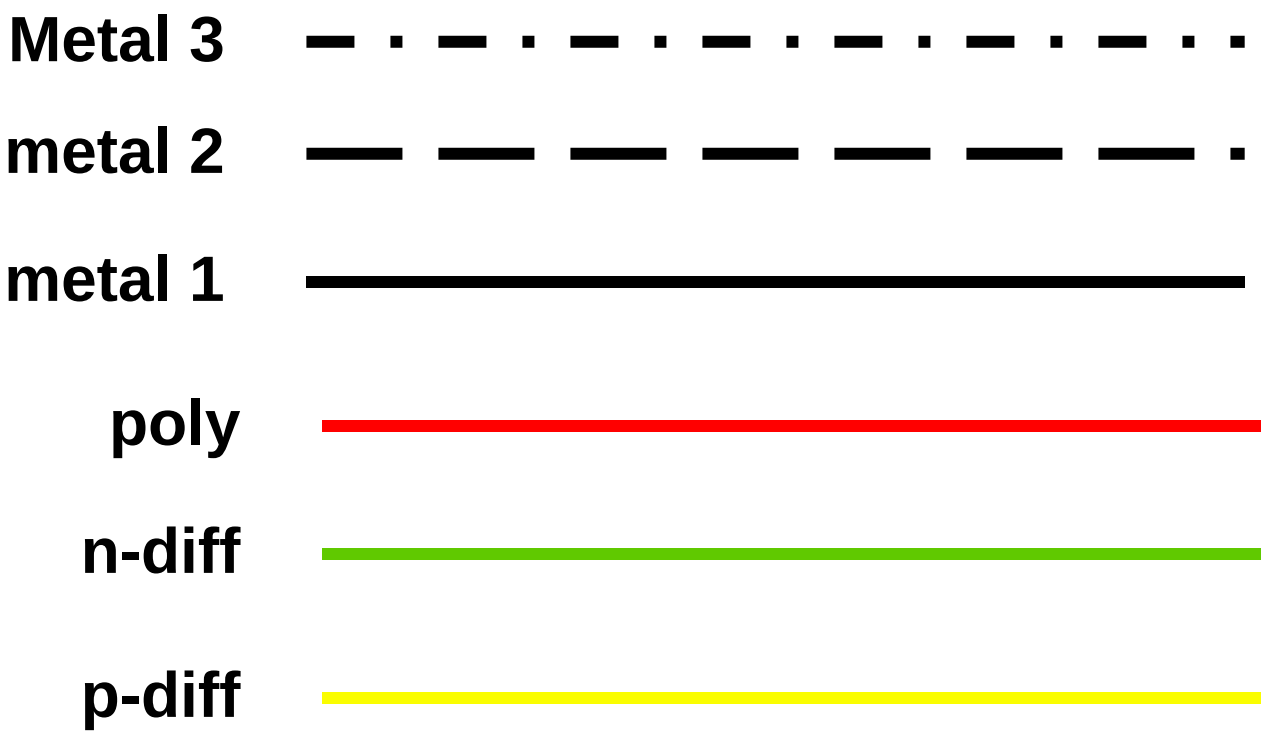
Layout



Stick diagrams

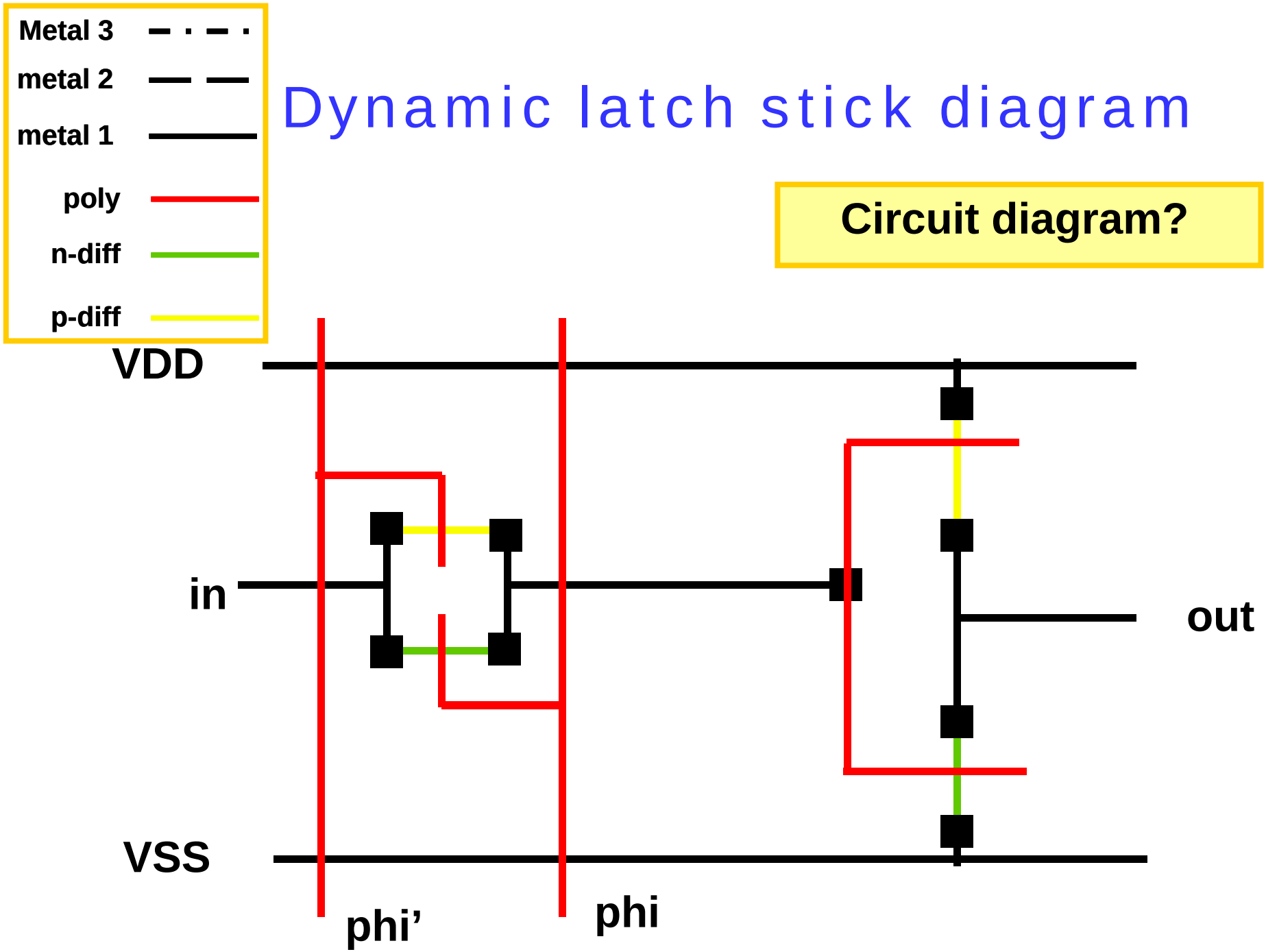
- **A stick diagram is a cartoon of a layout.**
- **Does show components/vias but only relative placement.**
- **Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries, some special components.**

Stick layers



- **Caution: stick diagrams don't display wells, use different colors for active area to distinguish between n-diff and p-diff**

Dynamic latch stick diagram



Exercise

See transistor layout below.

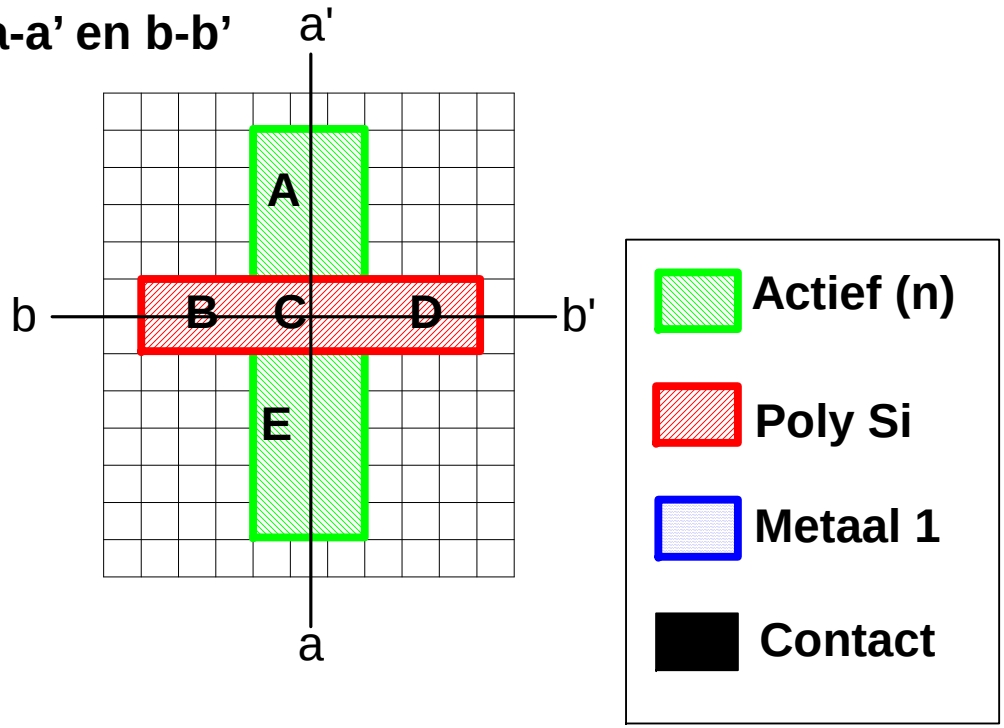
Determine for each of gate, source, drain which regions A-E (see the layout) form this terminal.

G: .....

S: ......

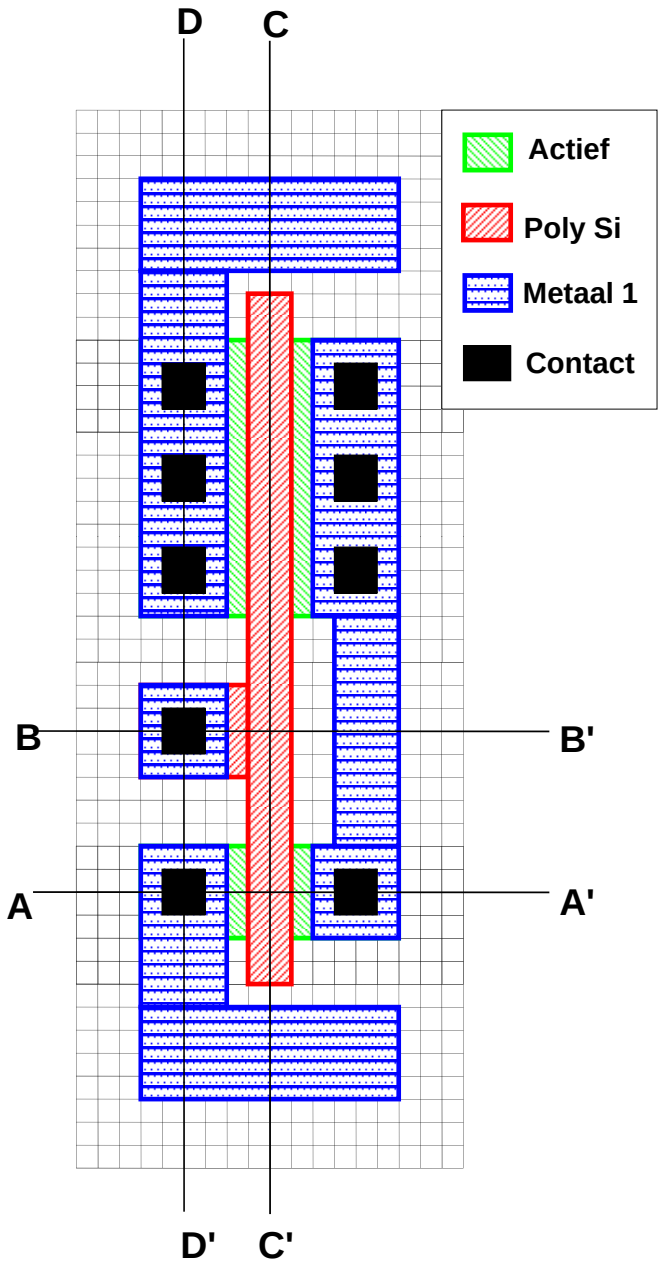
D: .....

Draw a cross-section through a-a' en b-b'



See the CMOS inverter layout on the right

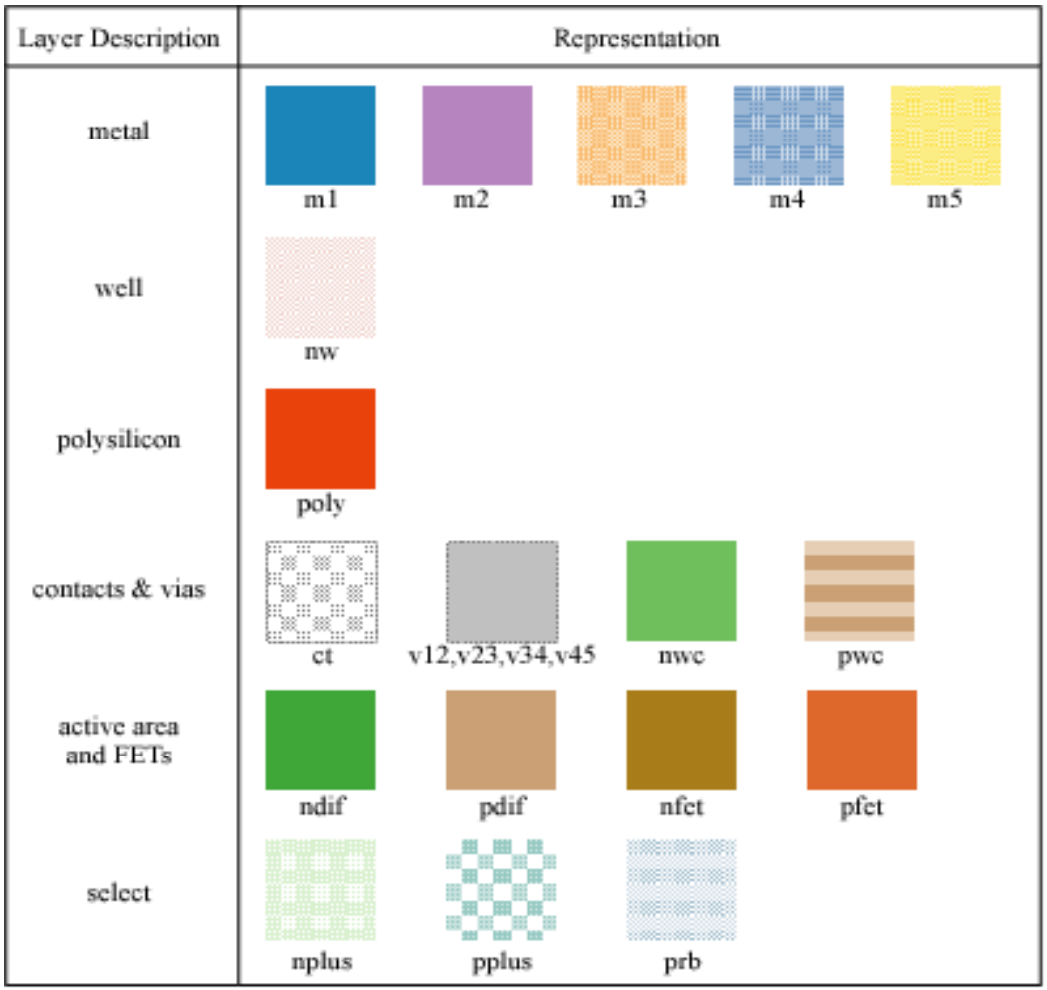
- Draw cross-sections A-A', B-B' and C-C'
- Which of the 2 transistors must be the P-transistor? Why?
- Draw the corresponding N-well.
- Annotate in the layout the location of the VDD and VSS terminals.
- Draw the schematic, including L and W ratios.



Design Rules

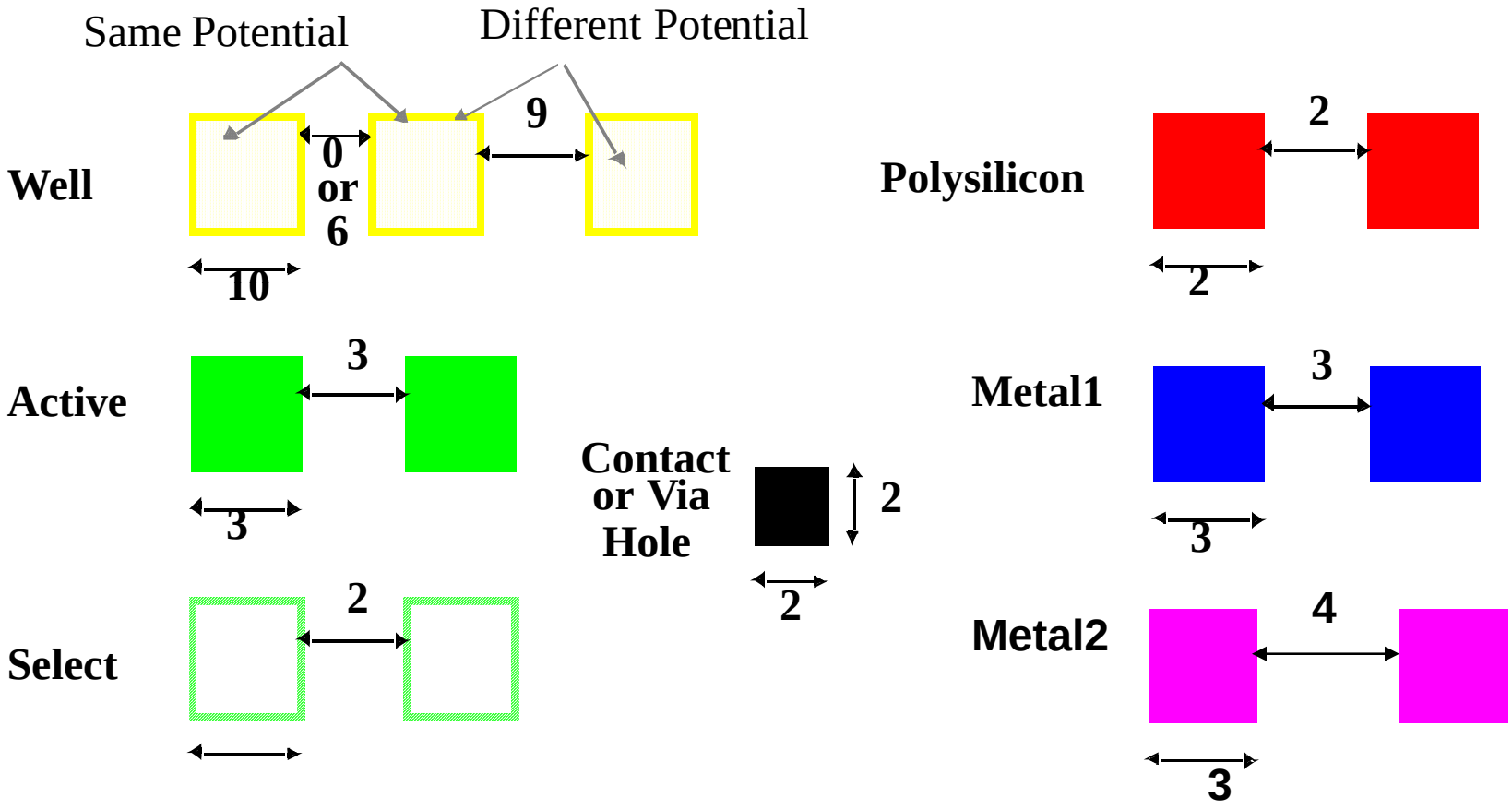
- **The fabrication process will suffer from tolerances**
- **Chip features will have a practical minimum size to allow them to be fabricated reliably enough (with high enough yield)**
- **This is captured into a set of precise Design Rules**
- **Modern processes have terribly complex set of design rules as a compromise between flexibility and manufacterability**
- **Need to work with those rules during cell layout.**

Layers in 0.25 μm CMOS process

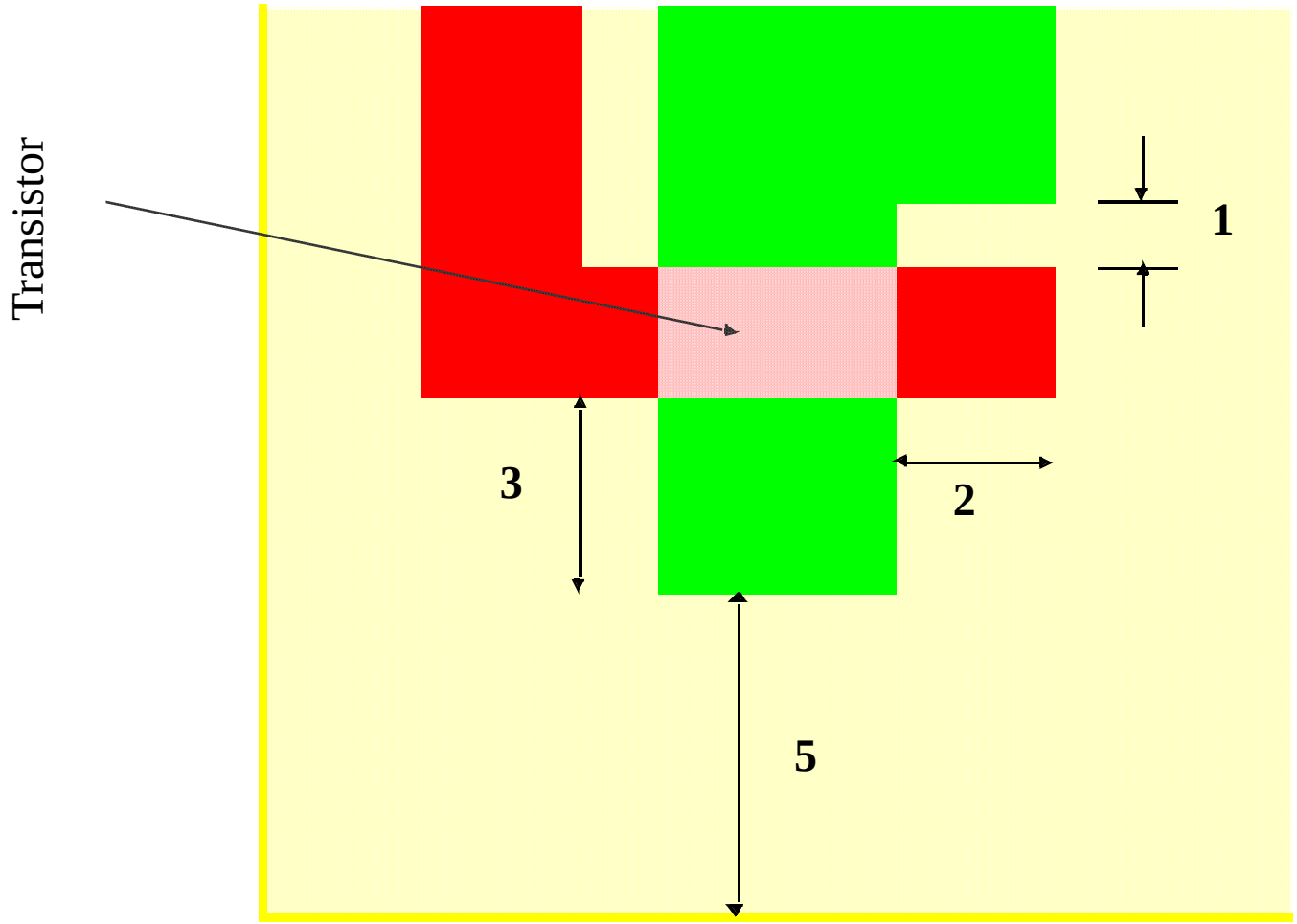


Intra-Layer Design Rules

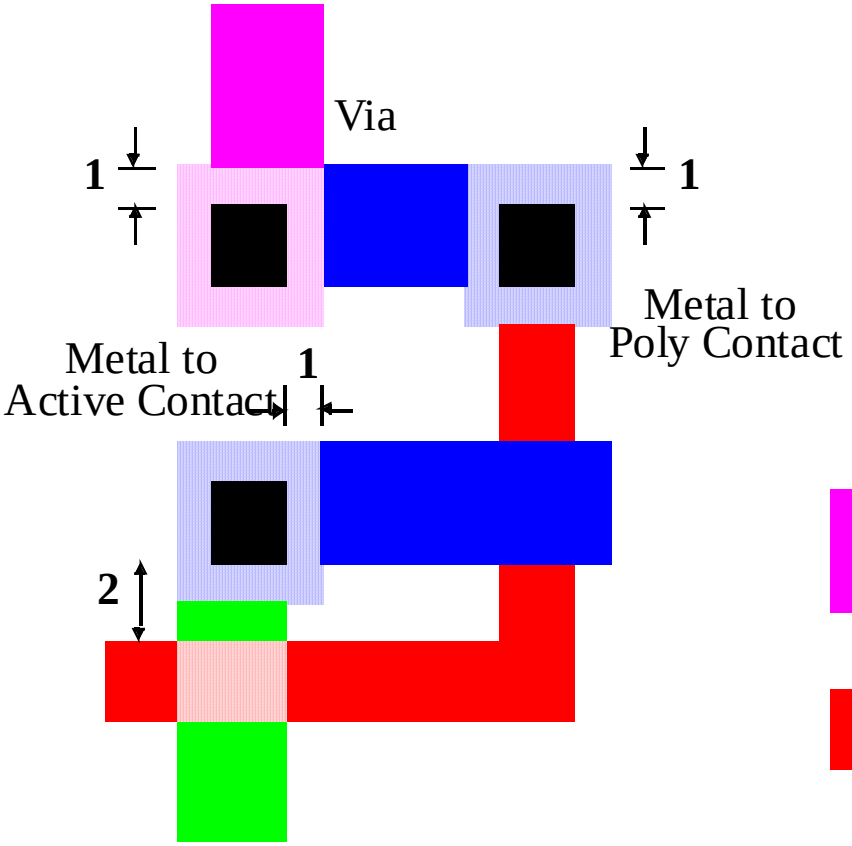
Example Rules

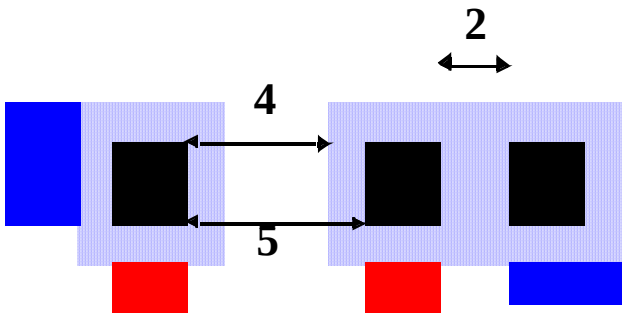


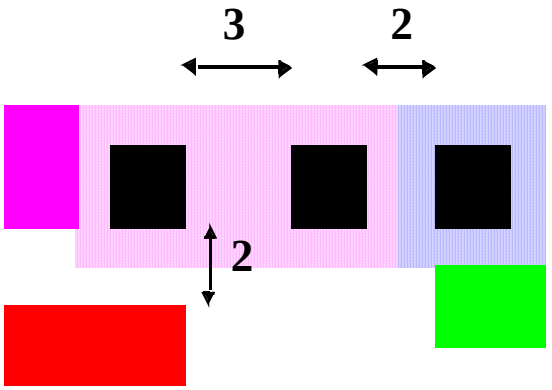
Transistor Layout



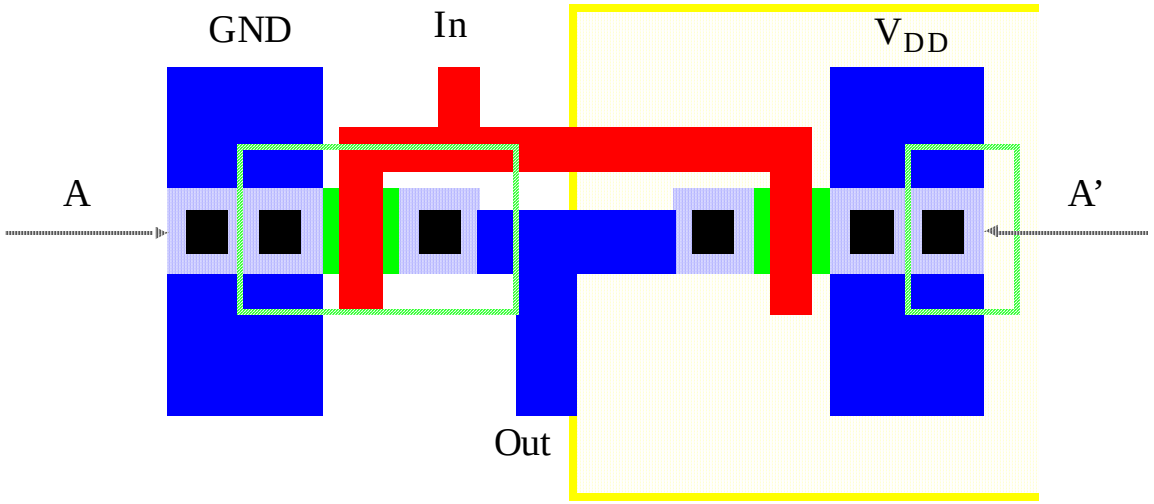
Vias and Contacts



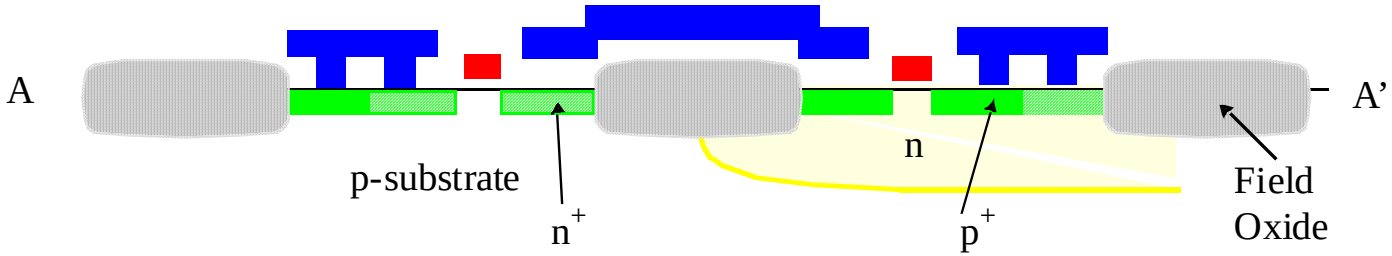




Inverter Layout and Cross-Section

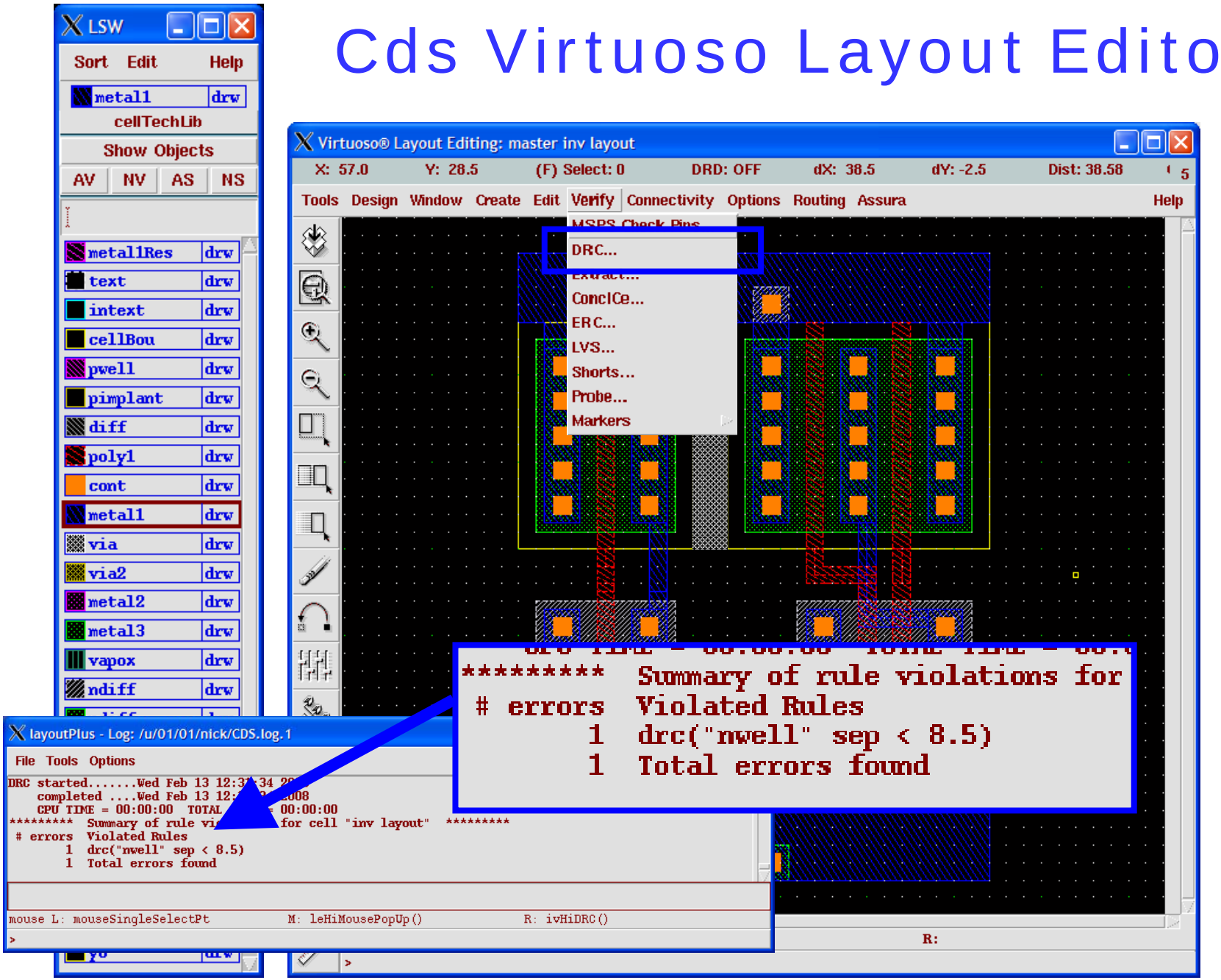


(a) Layout



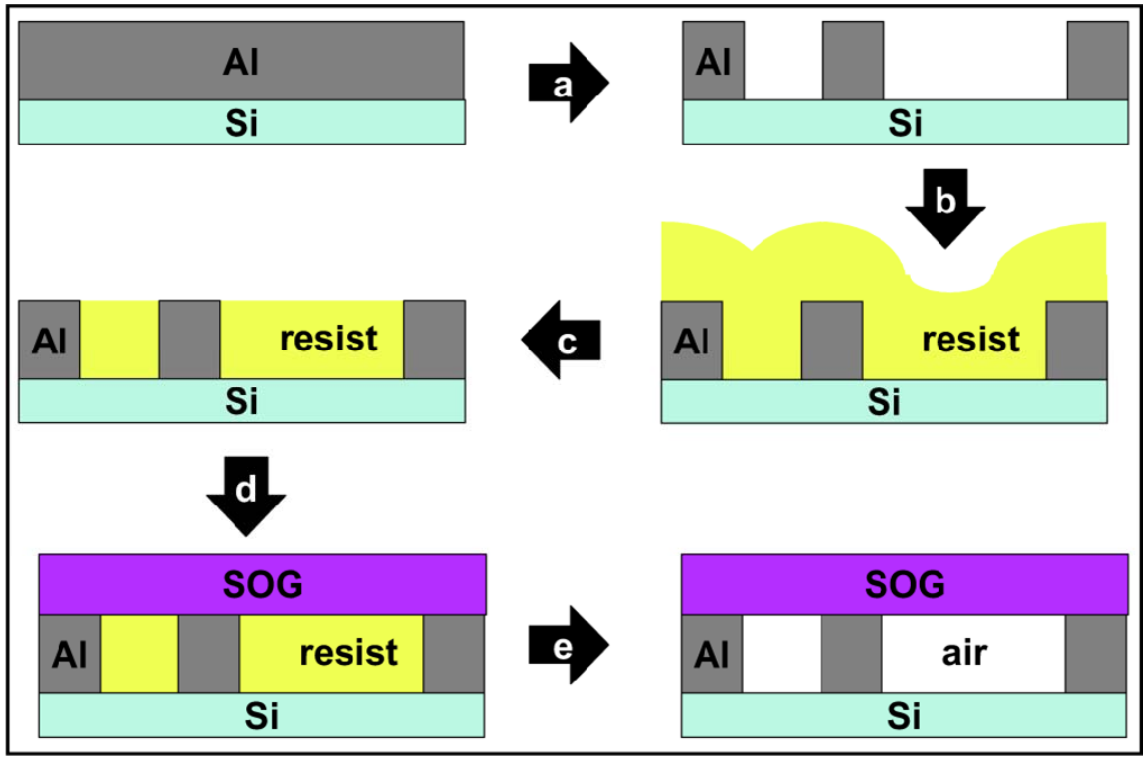
(b) Cross-Section along A-A'

Cds Virtuoso Layout Editor



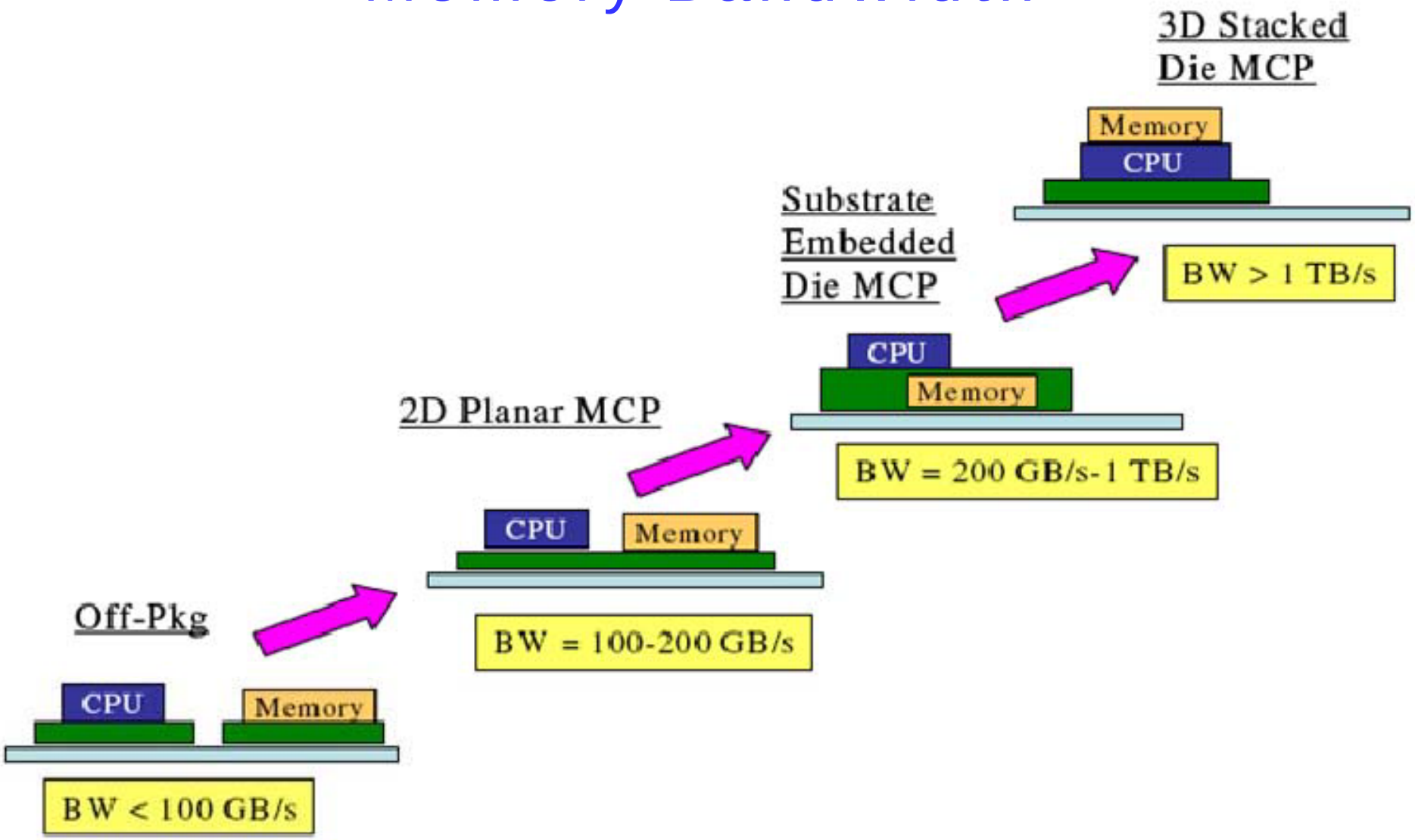
New Developments

- High-k for devices
- Low-k for interconnect
  - Even air-gaps →
- 3-D integration



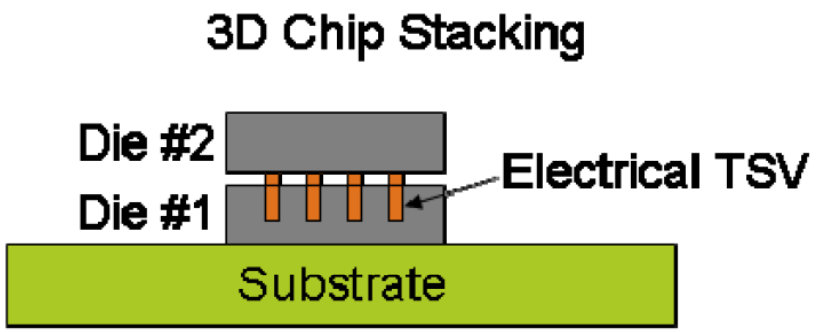
[Daamen, Journal of Microelectronic Engineering, 2007]

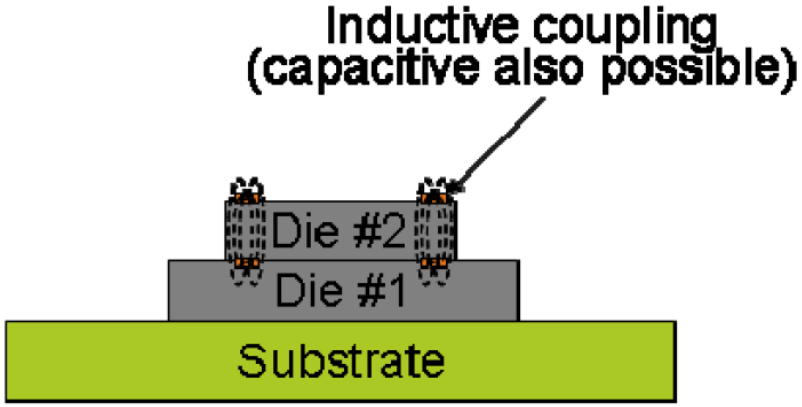
Memory Bandwidth

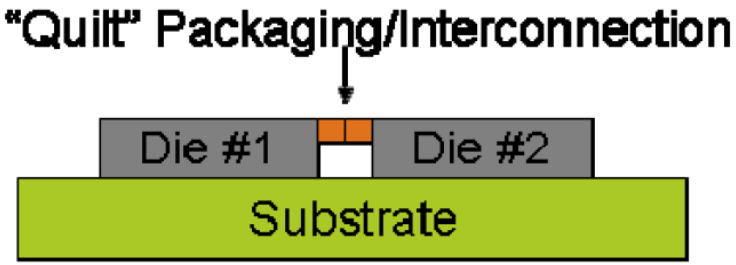


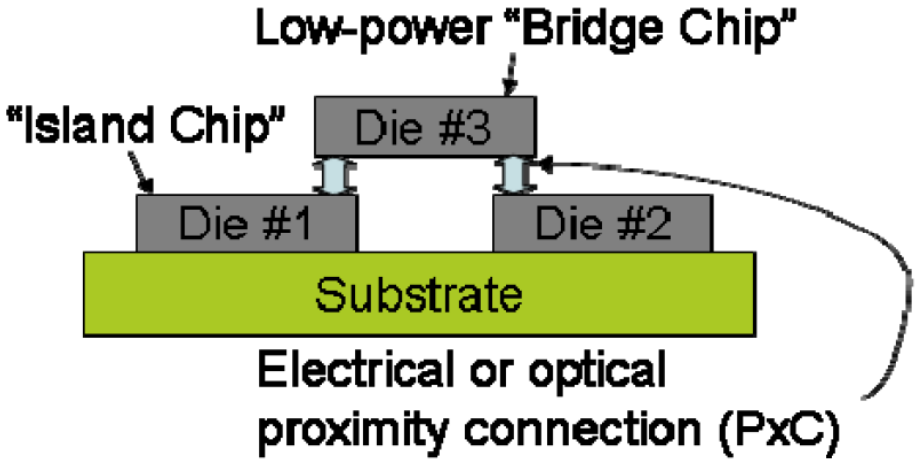
[Intel Technology Journal, vol 13, no 4, 2007]

System Interconnection



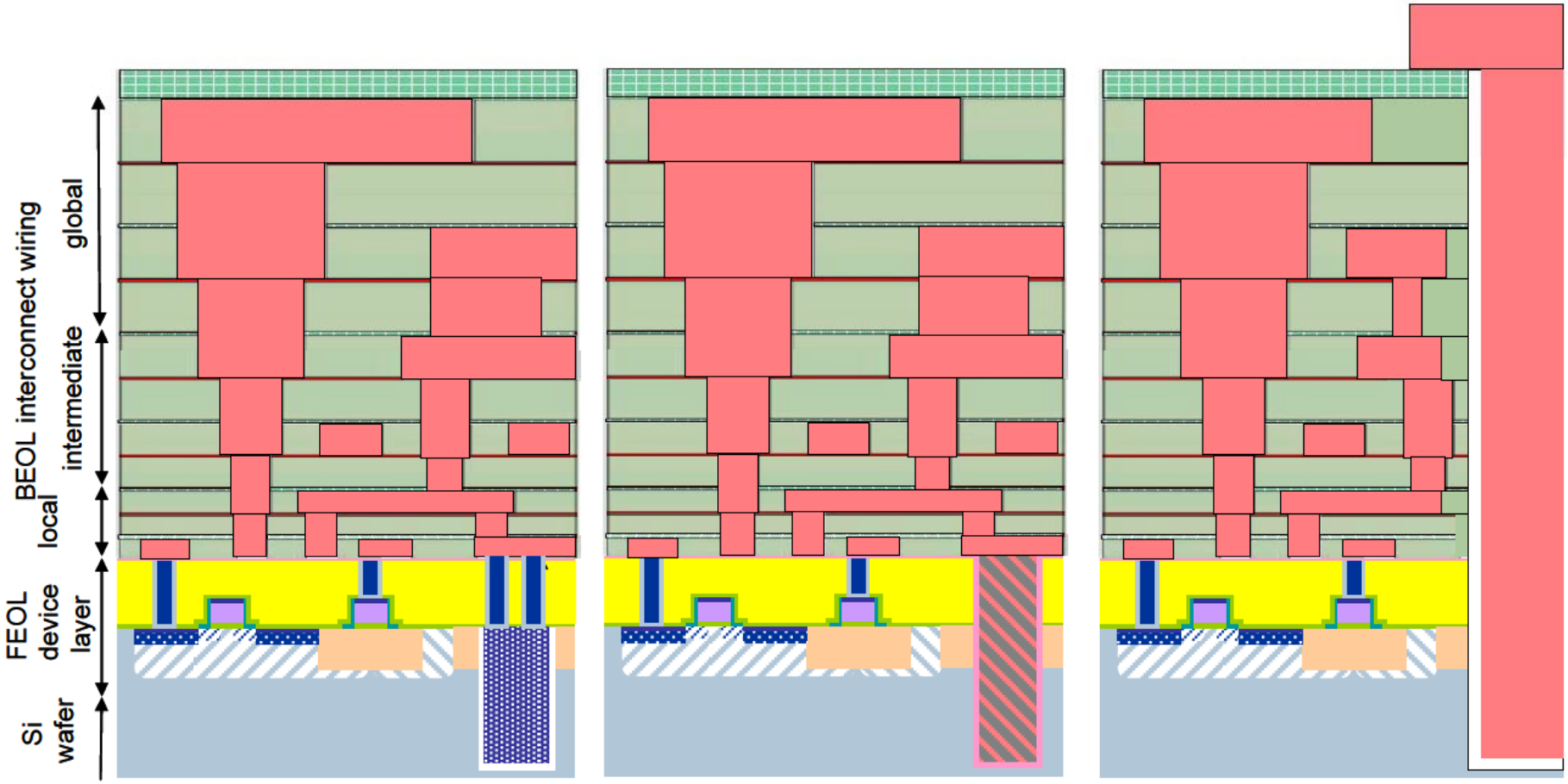






[ITRS 2009]

TSV Architectures



Via First **Via Middle** **Via Last**

[ITRS 2009]

Summary

- CMOS Processing
  - Photolithography
  - Material Deposition & Removal
  - Oxide Growth & Removal
- CMOS Process Outline
- Layout Design
  - Layer map
  - Layout examples
  - Stick diagrams
- Design Rules
  - Why we need design rules
- Technology continuous becoming more complex