ET4293 - Virtuoso Layout Design 2012

Instructions for the layout assignment in the Course Digital IC Design ET4293

Delft University of Technology

Course Year 2011-2012

http://ens.ewi.tudelft.nl/~nick/courses/digic/

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The basic steps of using the Cadence layout editor called Virtuoso will be covered. Some exercises are beneficial to gain a deeper insight into the fabrication process. This document is supposed to be a general overview of tool for beginners who haven't designed any layout before. The fundamental steps to design a PMOS device are used as an example.

Before starting, there are several things that must be set up. The following steps will guide you in this process:

1. Create your working directory and copy some files

>> **tcsh**

>> **cd /home/<username>**

Go to the directory where you want to create your working directory. You can select it, it's up to you!

>> **cp -r /opt/cad/cadence/5.1.41/sun4v/IC5.1.41/tools.sun4v/dfII/samples/tutorials/le/cell_design .**

Copy *cell_design* to the current directory and then use it as your working directory. Do not forget the "." at the end of the command line.

>> **cd ./cell_design**

Set *cell_design* as your working folder. The following steps will be operated from this directory.

>> **cp -r /opt/cad/cadence/5.1.41/sourceme .**

>> **vi sourceme**

Copy *sourceme* file to your working directory and open it with **vi** editor. Press the '**i**' key to edit it. Add the following line at the beginning of the file:

set path = ($path /opt/cad/cadence/5.1/lnx86/MMSIM701/tools/bin)

When you are done, press '**Esc**', and then type '**:wq**' to save the changes and leave the editor.

NOTE: You can use any kind of editors, like vim, gedit or emacs.

>> **cp /opt/cad/cadence/DesignKits/UMC090_ET4293/designkit/display.drf .**

Copy display.drf file to your working directory.

>> **vi cds.lib**

Open cds.lib with **vi** editor. cds.lib is an important file which specifies library information. It was copied to your project directory by the 'cp –r … cell_design .' command above. What we will do here is to add the library 'UMC090'. As before, press the '**i**' key to edit the file and add the following line at the beginning of the file:

include /opt/cad/cadence/DesignKits/UMC090_ET4293/designkit/cds.lib

When you are done, press 'Esc', and then type '**:wq**' to save the changes and leave the editor.

NOTE: You can use any kind of editors, like vim, gedit or emacs.

After following these steps, you will be ready to open the Cadence environment. Alternatively you can download the sourceme and the cds.lib files from:

http://ens.ewi.tudelft.nl/~nick/courses/digic/CadenceLocalGuide.html

2. Open ICFB

>> **source sourceme**

>> **icfb &**

Now cadence is activated by the command '**icfb &**' and a **CDS.log** window (Fig 1) pops up.

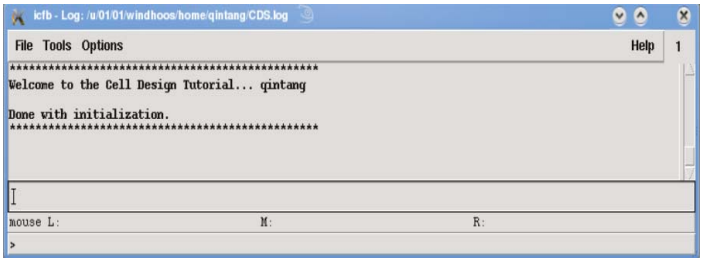

Fig 1. CDS.log window of icfb

3. Create your library

Start "library manager" (**Tools->Library Manager**), then create your own library by clicking **File→New→Library.**

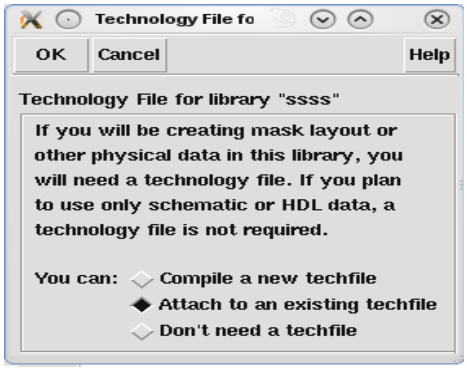

Fig 2. CDS.log window of icfb

The first thing to do is to type the name of the new library ("ssss" in this example). After entering

the name and clicking OK, a new window will pop up ('Technology file' window). Select here 'Attach to an existing techfile' and press OK. Finally, you will see the following window:

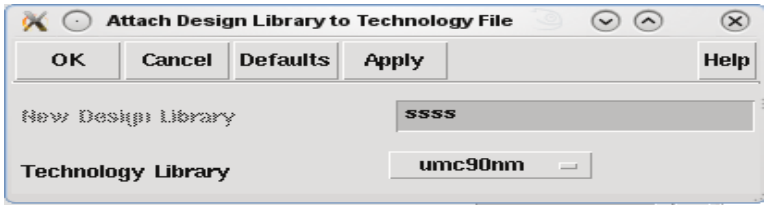

Fig 3. Attach Desing Library to Tech file window

Make sure you set Technology Library to **UMC090** (as in the figure above) and press OK.

4. Start the layout design

Select your library and click at: **File→New→cell view**. A new window, like the one at Fig 4, will pop up:

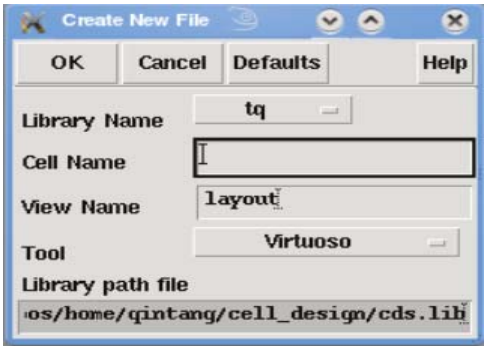

Fig 4. Create New File window

Type the cell name, and choose '**Virtuoso**' as Tool. Click OK and the Virtuoso Layout Editing window will pop up along with a **LSW** window, as shown in Fig 5. Description of various mask layers can be found at: /opt/cad/cadence/DesignKits/UMC090_ET4293/designkit/stream.map

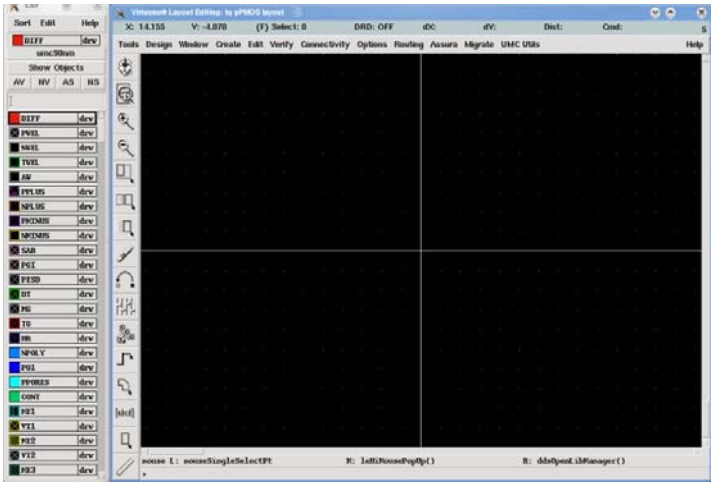

Fig 5. Layout Editing and LSW window

5. The layout design

The first thing you should do after starting the layout is fix the grid sizing. Go to **Options→Display**, or press the '**e**' key which is the shortcut for that, and the options window (Fig 6) will pop up. The **X/Y Snap Spacing** parameter is a foundry limitation resulted from the ability to place masks on the wafer, if you make a smaller grid, probably when you check DRC of the layout you will find lots of errors about 'offgrid', if you don't correct this errors the foundry will refuse your fabrication order. The default value 0.005 is fine. Click OK to save your changes or just keep the defaults.

Fig 6, Setting options for layout design

After setting up the options go back to the Virtuoso Layout Editing window (Fig 5). In the left column window, you can see the icons for **Save, Fit Edit, Zoom in, Zoom out, Stretch, Copy, Move, Delete, Undo, Properties, Instance, Path, Polygon, Label, Rectangle and Ruler**. You will use them frequently during designing. The short-cut keys listed below will help you work faster. Take '**r**' as a case, before you draw any layer, you should select corresponding layer from the **LSW** palette window, click it then move the cursor to **Virtuoso Layout Editing** window to left-click so as to activate it. Press '**r**' on the keyboard or click the icon for **Rectangle**, sequentially left-click and drag the mouse pointer to define the range. After drawing, ***do remember to press Esc to exit this mode***. Detailed explanations for these commands are listed below.

Edit Menu Commands

Rectangle	Create a rectangle of the selected layer in the LSW.
Move:	Click on any object and move it around in the layout.
Stretch:	Click on the edge of a rectangle and size it. Be careful during using it. Before using it, make sure no object is selected; otherwise the selected object in your previous step will be moved unexpectedly.
Path:	Create a path of the selected layer in the LSW. *(Double click to end the path).*
Undo:	Undo the previous commands.
Copy:	Create a copy of any object in the layout.
Properties:	Change the properties of objects in the layout. Change the layer definitions and the changes are immediately reflected in the layout.
Instance:	Import another existing cell view into this cell view.

Shortcuts

- r	Create a rectangle	- m	Move
- s	Stretch	- p	Create path
- u	Undo	- c	Copy
- k	Ruler	- q	Show properties
- i	Add instance	- SHIFT+z	Zoom out
- f	Fit the whole design on the screen	- CTRL+z	Zoom in

NOTE: To zoom in/out in the schematic, use the mouse wheel.

For this laboratory session our first goal is to design a PMOS transistor. PMOS transistors are built in an Nwell, which is put in the P-type substrate. The black background in **Virtuoso Layout Editing** window can be considered as the P-substrate so NMOS device can be put directly in it while PMOS devices need Nwell. Fig 7 shows the different layers required to build a PMOS transistor while Fig 8 shows a completed design. A detailed explanation of the PMOS layout design can be found in the **Appendix** section. A PMOS transistor is composed of these layers listed below (names are from LSW window):

NWELL	P01 (polysilicon)
PPLUS (S/D P+ implant)	CONT (contacts)
SDSYM	DIFF (S/D diffusion, active region)
DEVICE	ME1 (metal layer 1)

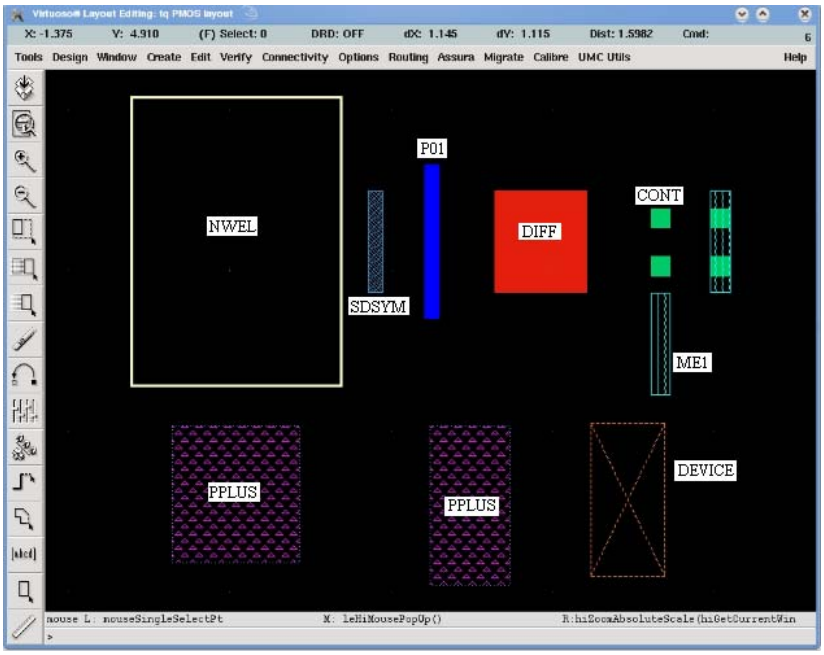

Fig 7. PMOS transistor building layers

Fig 8. PMOS layout

When you're designing layout, the most important thing you should keep in your mind is the DRC rule. The design rules are specific for particular manufacturing processes, which set certain geometric and connectivity restrictions to ensure that most of design works correctly. If you don't comply with it, you will face numerous errors and warnings after DRC. That's terrible! The most frequently used rules are illustrated in **Layout_rules.ppt**. Please read them and refer to them during designing.

Maybe you will be wondering: why there isn't any N-plus layer to connect the Nwell to a high voltage. Generally designers will design the M1-NWEL and M1-Psub contact models to connect the Nwell and substrate to metal respectively. As a result, the PMOS and NMOS models are simplified and compact.

6. DRC (Design Rule Checking)

DRC is available with Cadence distribution which checks most of the rules. The next step following with completing layout design is to run DRC to ensure the designed layout meets the design rules and therefore can be manufactured. There are two methods to run DRC, one is Assura and the other is Calibre. Calibre will be used in this laboratory session. However, there is no Calibre menu at the Virtuoso Layout Editing window.

In order to make it available we need to edit **.cdsinit** and **sourceme** files, so let's exit icfb, and download these two files from:

http://cobalt.et.tudelft.nl/~nick/courses/digic/CadenceLocalGuide.html

to your working directory to overwrite the old ones. Next we need to do some additional modifications:

>> **cp -r /opt/cad/cadence/DesignKits/UMC090_ET4293/designkit/RuleDecks/Calibre ..**

Copy the Calibre directory to your working directory.

>> **cd ../Calibre/DRC**

Change to Calibre/DRC as the working directory.

>> **pwd**

This instruction shows the absolute path for our working directory (you will need it later).

>> **vi G-DF-LOGIC_MIXED_MODE90N-1P9M2T1F-Calibre-drc-1.4-p1**

Open the file using the **vi** text editor. Here we need to edit some lines to make the DRC work properly. To jump to a specific line type "**:#line**", where *#line* is the line number you want to access. Type '**i**' to edit the text and press '**Esc**' to stop editing. You need to edit the following lines:

- **Line 291:**

  BEFORE: INCLUDE ./90nm_layers_v3.8.cal

  AFTER: INCLUDE <*path*>/90nm_layers_v3.8.cal

- **Line 9238:**

  BEFORE: INCLUDE ./umc_1P9M2T1F-X_architecture_Calibre-drc-V1

  AFTER: INCLUDE <*path*>/ umc_1P9M2T1F-X_architecture_Calibre-drc-V1

- **Line 9246:**

  BEFORE: INCLUDE ./umc90N_memory_v14.cal

  AFTER: INCLUDE <*path*>/umc90N_memory_v14.cal

Where <*path*> is the absolute path of the Calibre/DRC directory you got after typing the **pwd** command.

When you are done press '**Esc**' and '**:wq**'.

NOTE: you can use any kind of editors, like vim, gedit or emacs.

Go back to your design directory and next execute s**ource sourceme and restart icfb**. This time you will be able to see the **Calibre** menu in your layout if you followed the steps correctly.

Note: .cdsinit is a hidden file; you can read it by command 'cat' in x-term or set up your computer not to hide files.

1. Open your layout window, and select **Calibre→Run DRC** to invoke the **Calibre Interactive – nmDRC** window (Fig 9). If this is the first time for you to run DRC, click **Cancel** at **Load Runset File** (if you saved a runset file before and you want to load it, specify the runset file here). Specify DRC Rule File and DRC Run Directory as it is shown in Fig 10. The DRC Rule File can be found in the local **Calibre/DRC** directory. The rule file name is:

   G-DF-LOGIC_MIXED_MODE90N-1P9M2T1F-Calibre-drc-1.4-p1

2. Specify the 'Top Cell' (Fig 11). If you need to change some DRC switches, you have to edit the Calibre DRC file.

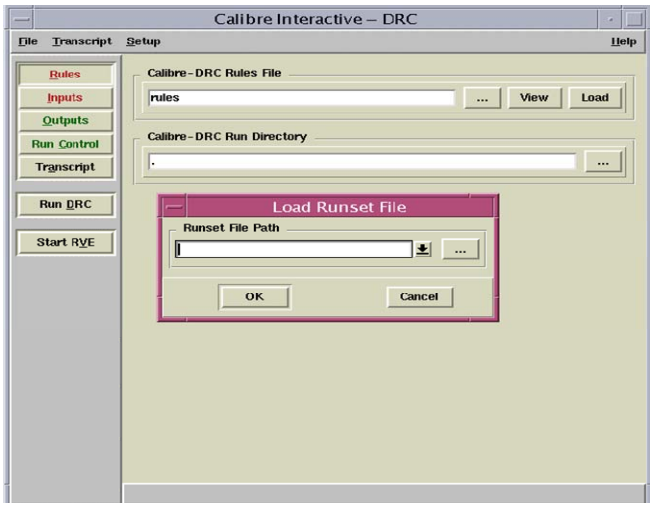

Fig 9. Calibre Interactive – nmDRC window

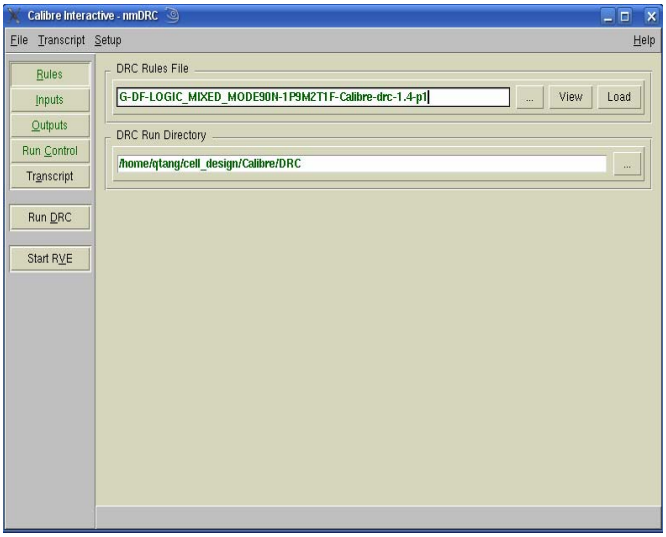

Fig 10. Specifying the DRC rule file and run directory

3. Click **Run DRC** icon on the left of **Calibre Interactive – nmDRC** window. Finally you will have **Calibre – DRC RVE** and **DRC Summary Report** windows with design rule violations as indicated in Fig 12 and Fig 13 respectively.

4. Correct your layout according to the errors and warnings in **Calibre – DRC RVE** window (Fig 12). Click at the errors to get some information about it at the bottom of **Calibre – DRC RVE** window (Fig 12). At the same time, the location of error will be highlighted in the layout. It should be easy for you to realize what should be modified.

5. Repeat correcting layout and running DRC until there is no error shown in **Calibre – DRC RVE** window (Fig 12). However, if there are errors like

   - **Minimum DIFF density over 150m*150um area step 50 is 25%**
   - **Maximum P+ diffusion to nearest N+ pick-up spacing is 20um**

that you can ignore. The former arises because it's just a small model. The latter is due to the Nwell contact (if the PMOS model were used, there should be an Nwell-Metal contact to connect Nwell to the supply voltage).

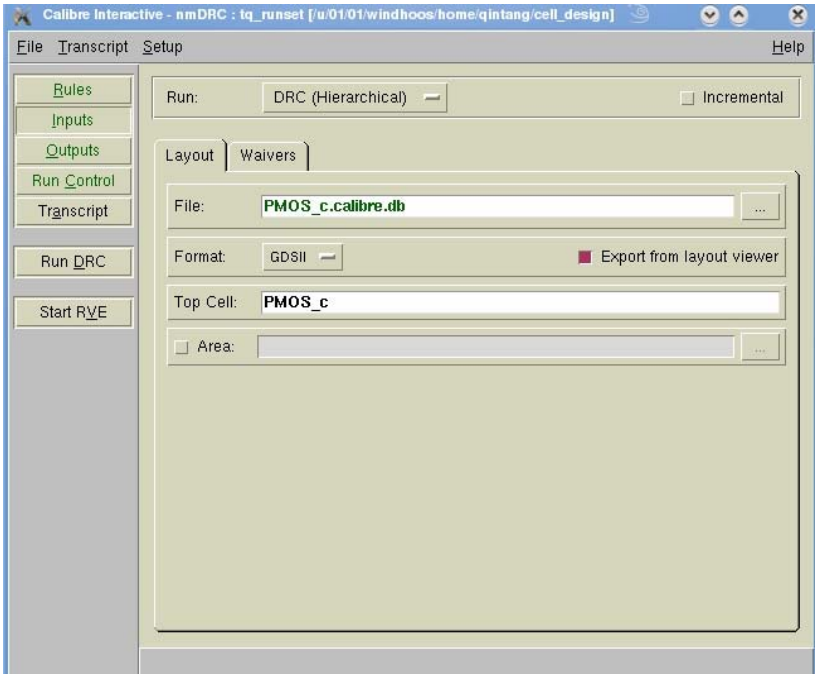

Fig 11. Specifying the top cell

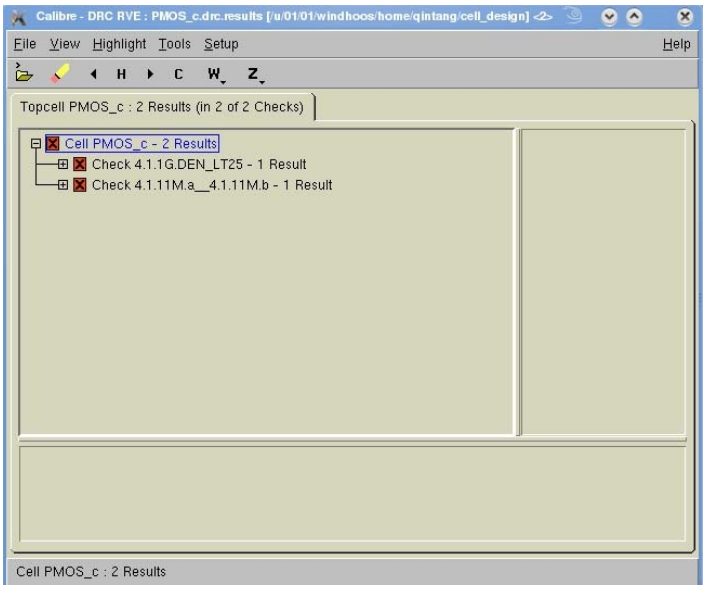

Fig 12. Calibre-DRC RVE window

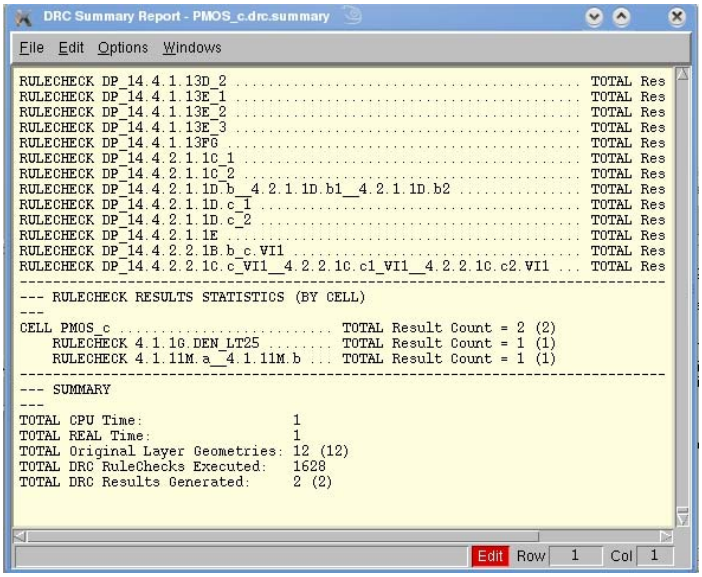

Fig 13. DRC Summary Report

The next step is to run LVS (Layout Versus Schematic) to ensure that the schematic matches the corresponding layout. This part is not covered here.

One example to layout correction according to DRC results

This is an example to show how to correct a layout in order to make sure everything you place in the layout is compliant with the design rules. For this example, I modified the layout (Fig 14) and ran the DRC, whose results are shown in Fig 15. By clicking at **Check 4.1.13C.a-2 Results** and then double-clicking at **01**, you can see the error is highlighted and amplified in the **Layout Editing** window. The bottom of **Calibre – DRC RVE** window shows the information about the error:

Minimum spacing of DIFF CONT to P01 is 0.08um / P01 with width <= 0.13um.

which means the CONT in the left of Poly layer is placed too close to poly, the spacing between them must be at least 0.08um. So the two CONTs on the left are supposed to be moved towards the left. Finally, after editing the layout, and running the DRC again, the results indicates that there are only two errors (Fig 16). As said previously, these two kinds of errors could be ignored.

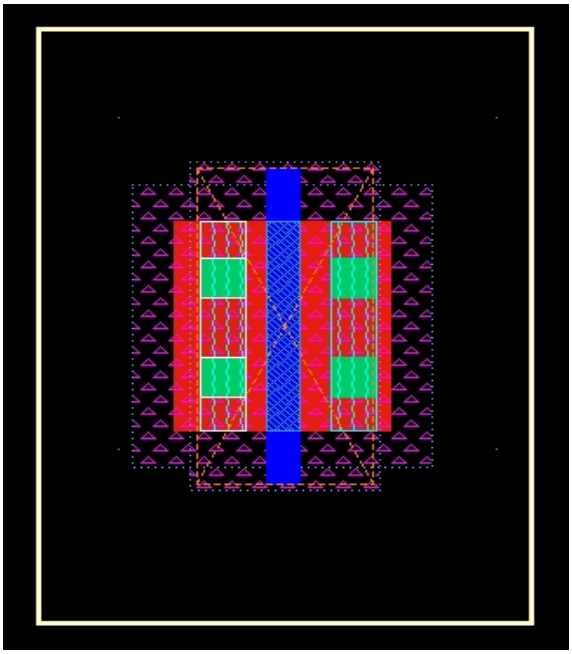

Fig 14, Modified layout view

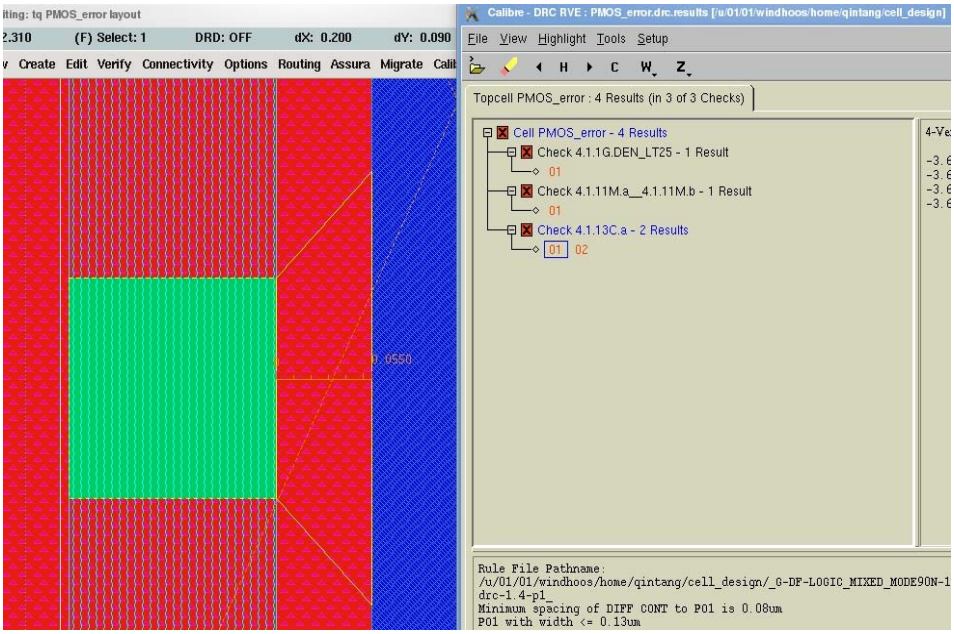

Fig 15. Highlighted error

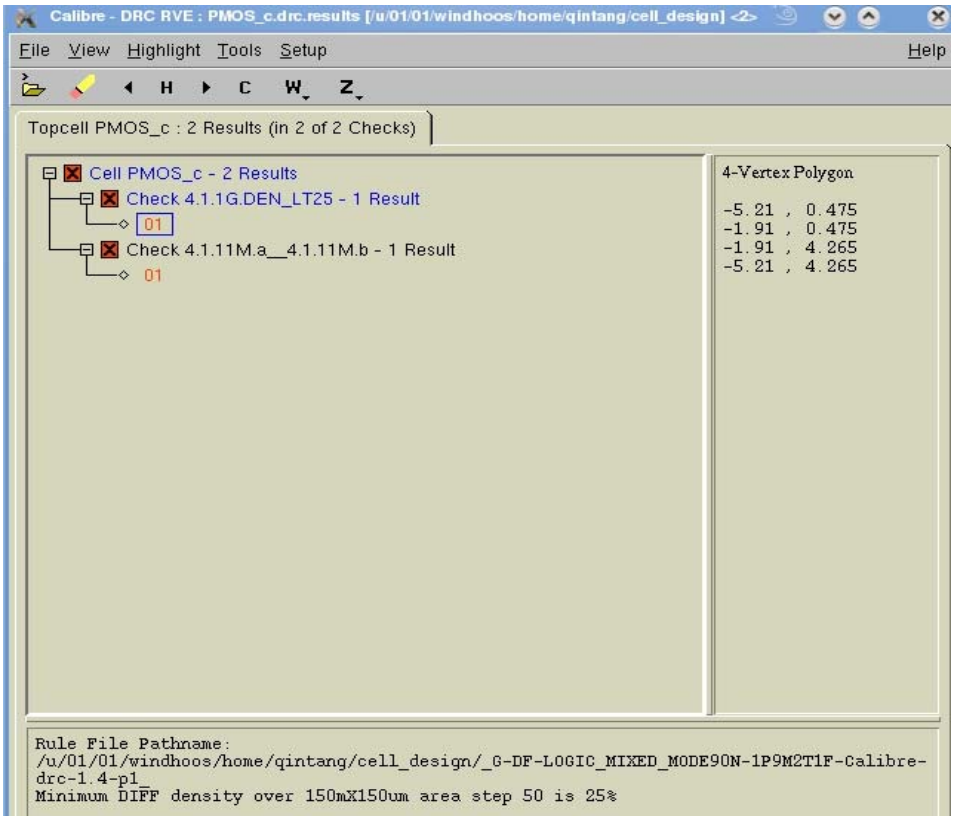

Fig 16. DRC results after correction

7. The design flow

When you want to design circuits, no matter how large and complicated they are, you should follow this design flow:

1. design the schematic
2. simulate the schematic to make sure the function meets the requirements
3. design layout
4. Physical verification (DRC, LVS, PEX)
5. Post-Layout Simulation

This part will introduce the first 4 steps with a simple inverter as a case. But the introduction of the forth step will focus on DRC, which has been explained in detail.

7.1. Design the schematic *inverter*.

In **CDS.log** window (Fig 1), open "library manager" (**Tools→Library Manager**). Click in your library and create a new cell view (**File→New→cell view**). At the "**Create New File**" window, fill in the cell name and select "**composer Schematic**" as Tool (Fig 17).

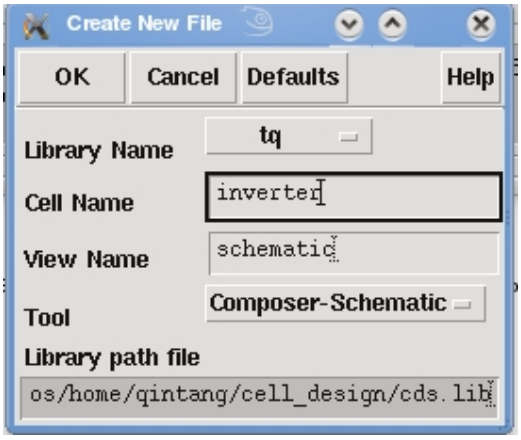

Fig 17. Create new schematic

After Clicking OK, the **Virtuoso Schematic Editing** environment will show up. Press the '**i**' key to add instances to the schematic and select NMOS and PMOS models from the Library UMC90 (Fig 18). Their width and length values will depend on the specific requirement. You should calculate them approximately and set these values manually.

Once the transistors are placed, select the voltage supply (Vdd) and ground (gnd) models from the **analogLib** library. Now it's time to connect them. Press the '**w**' key to connect these four models and add an input pin (**I** in this example) and an output pin (**O** in this example) by pressing the '**p**' key.

Note: press Esc after finishing every mode, then using icons or keys to enter new mode. & Click 'save' frequently, just in case of some unexpected situations. It's a good habit for designers.

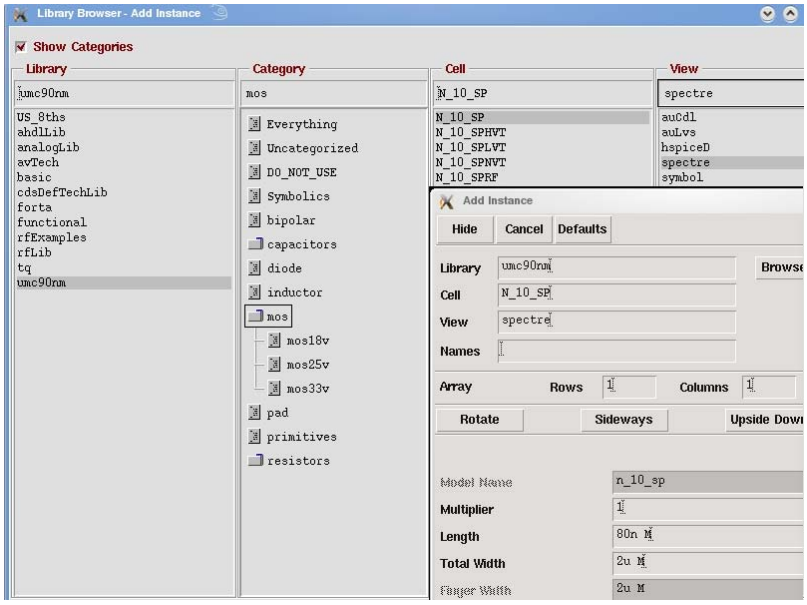

Fig 18. Adding NMOS spectre model

7.2. Simulate the schematic to make sure the function meets the requirements.

In order to simulate the inverter, we usually create a symbol for the inverter, and then create a new schematic named ‘inverter_test’, where the symbol of inverter is added.

Therefore, open the inverter schematic and click at **Design→Creat Cellview→From Cellview**. Click OK in the pop-up window (Fig 19), and also for next one. Finally **Virtuoso Symbol Editing** window will pop-up, where you can see the symbol of the inverter with the same names for its input and output ports.

Remember to save the file by selecting Design→Check and Save in the Symbol Editing window.

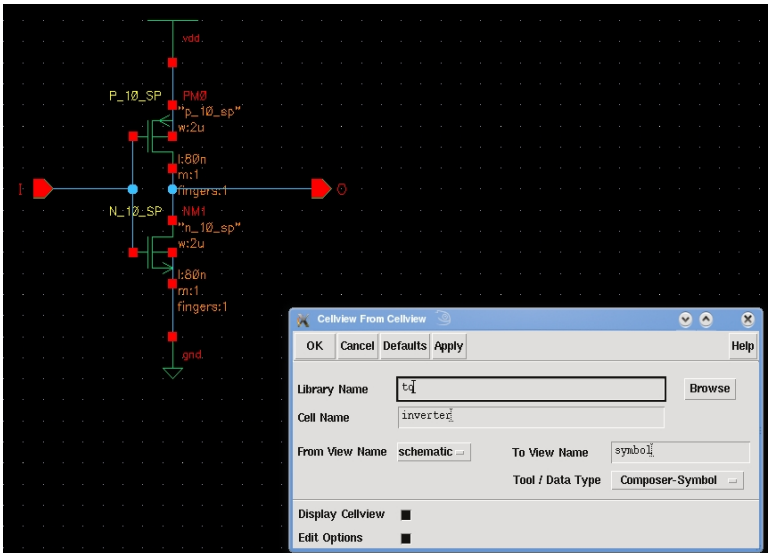

Fig 19. Creating a new symbol

Create new schematic named ‘inverter_test’, and add the inverter symbol from your library (‘**i**’ key). Place it in your schematic by clicking in the design space and press ‘**Esc**’ to exit. In the same way add a time varying voltage source (**vpulse**), a constant voltage source (**vdc**), a capacitor (**cap**), and Vdd and gnd models.

vpulse is selected from:

analogLib(Library)→Source-Independent(Category)→vpulse(Cell) →symbol(View)

Set up its values as shown in Fig 20:

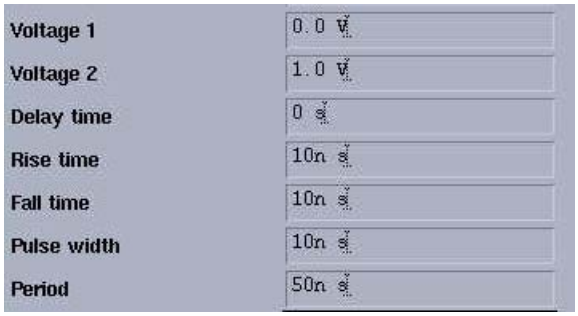

Fig 20. vpulse values set up

vdc is selected from:

analogLib(Library)→Source-Independent(Category)→vdc(Cell)→symbol(View)

Set up its value as shown in Fig 21:

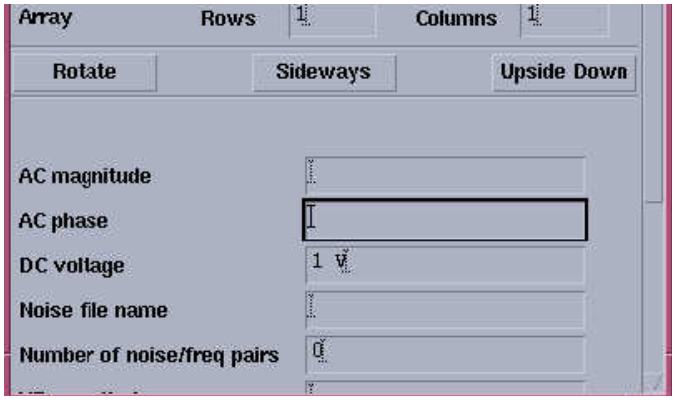

Fig 21. vdc set up values

cap is selected from:

analogLib(Library)→passive(Category)→cap(Cell)---symbol(View)

The final schematic for simulation is shown in Fig 22. By selecting a symbol and then pressing '**e**', you can check the sub-circuits this symbol is made of. To go back to the "parent circuit", press **'Ctrl+e'**. Any modification of *inverter* in *inerter_test* will be saved to *inverter*, so be careful.

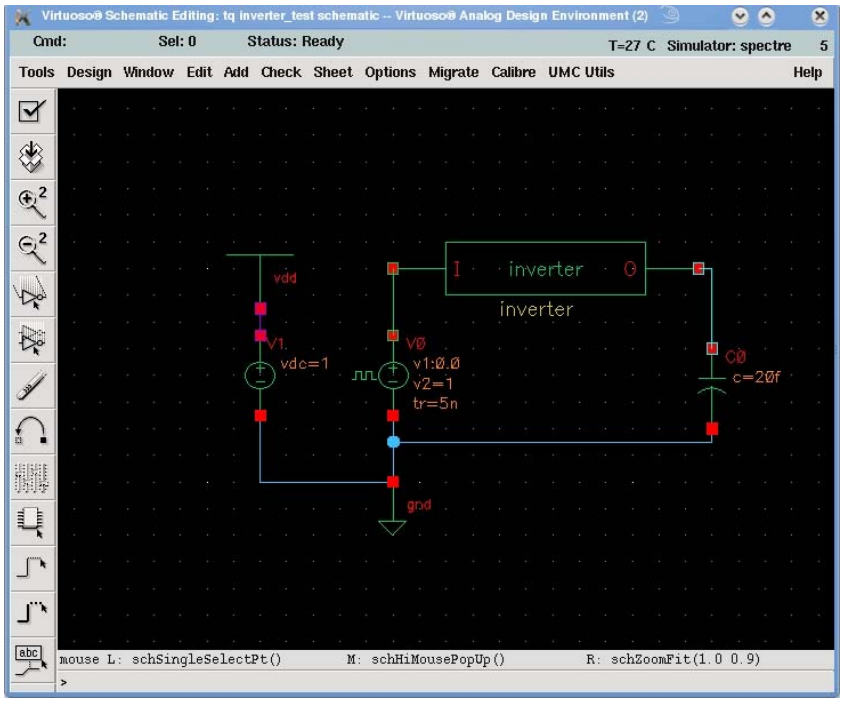

Fig 22. Complete schematic inverter_test

After connecting everything for test, click at **Tools→Analog Environment** in the **Schematic Editing** window which will show the **Virtuoso Analog Design Environment** window (Fig 23).

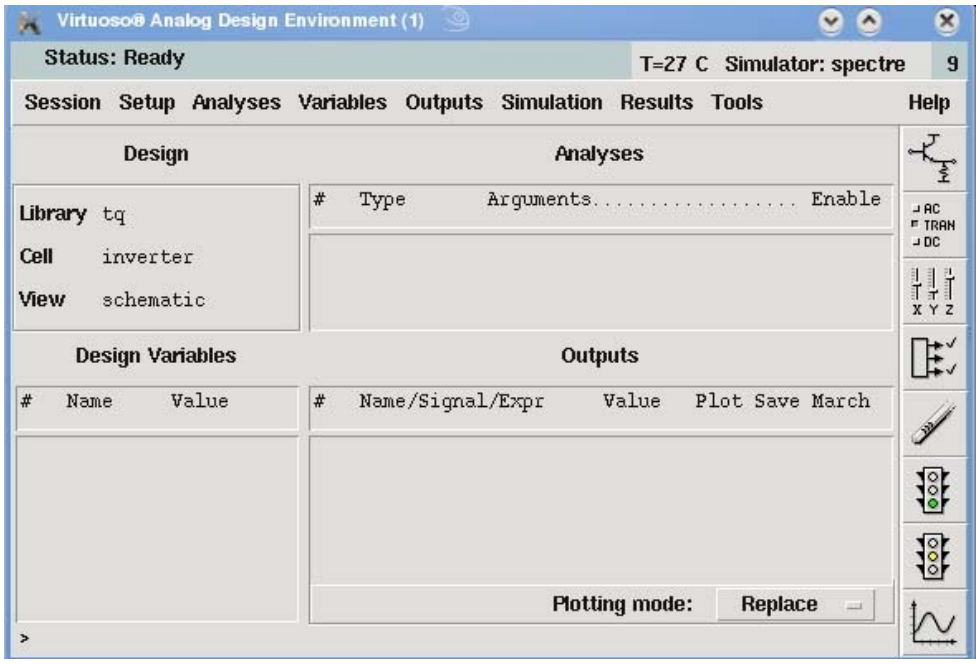

Fig 23. Analog Environment window

In the **Virtuoso Analog Design Environment** window, select:

Setup→Simulator/Directory/Host

The **Choosing Simulator/Directory/Host** window will appear (Fig 24). Make sure that the simulator is set to '**spectre**' and click on OK. Now go to **Analyses→Choose** and make sure it's set to "transient analysis" and provide an "end of simulation" time. Then click OK.

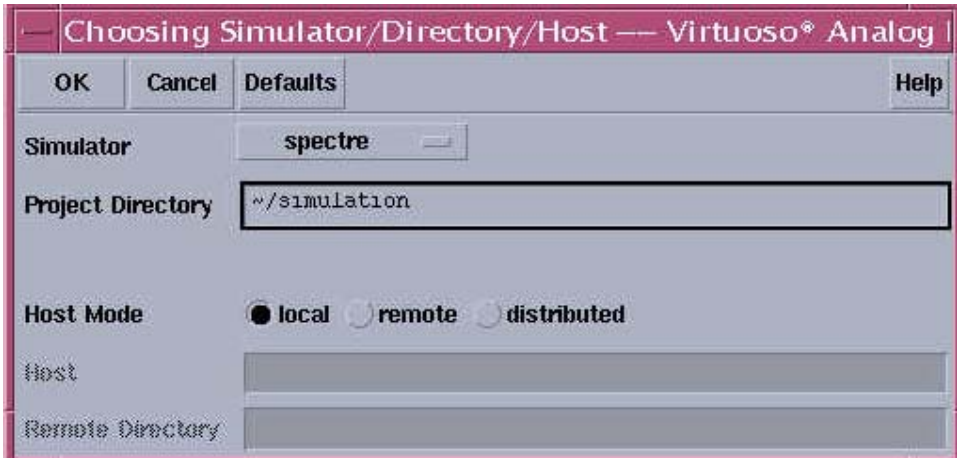

Fig 24. Setting up the simulator

In the **Virtuoso Analog Design Environment** window, select **Setup→Model Library Setup**. Check the model directories and you will have the same window as in Fig 25.

Select all those library files and click '**Disable**' on the right of **Model Library Setup** window. After that, select only the file named:

'…/designkits/umc90nm/…Models/Spectre/L90_SP_V051.lib.scs tt'

and enable it. Finally click OK to save changes.

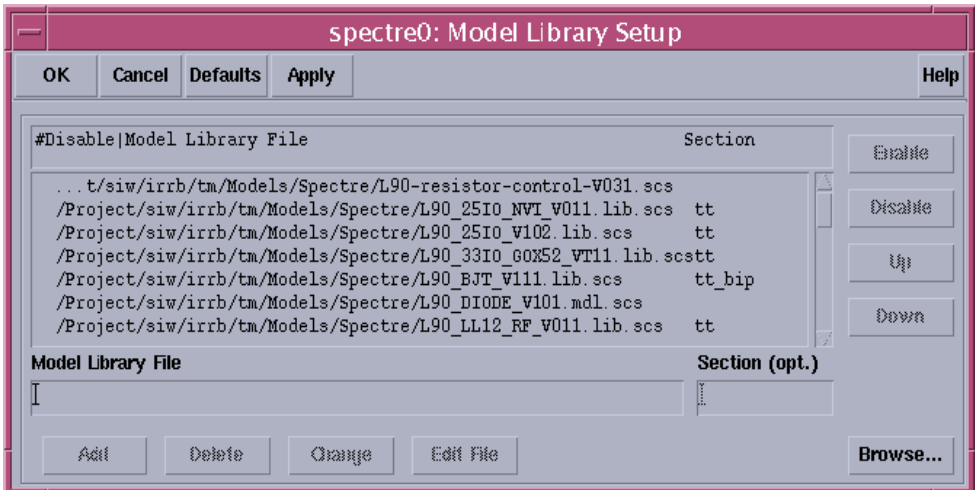

Fig 25. Setting up the model path

Please refer to http://www.ee.ucla.edu/~dejan/ee115c/ee115c_tut_2.htm to obtain more information about how to simulate a schematic design.

Modify the W/L ratio of NMOS and PMOS devices to meet specifications. The requirement of this year is to make the falling transition time and rising transition time equal. Modify W/L of NMOS and PMOS to see the dependence of output transition time on W/L ratio.

Once your design meets specifications, the next step after completing the schematic design is to design layout.

7.3. Layout design

The basic steps for PMOS layout design have been introduced in detail at the beginning of this paper. Now another method to design layout will be explained.

Open the *inverter* schematic and select **Tools→Design Synthesis→Layout XL**. You will see a Startup Option window (Fig 26). Select '**Create New**' and click OK.

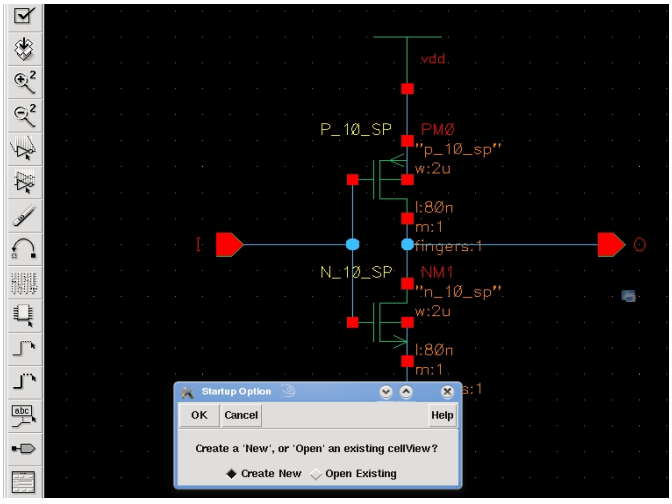

Fig 26. Startup Option window

A familiar window will pop up (**Create New File** window (Fig 27)). Click OK to get an empty **Virtuoso Layout Editing** window for the *inverter* layout.

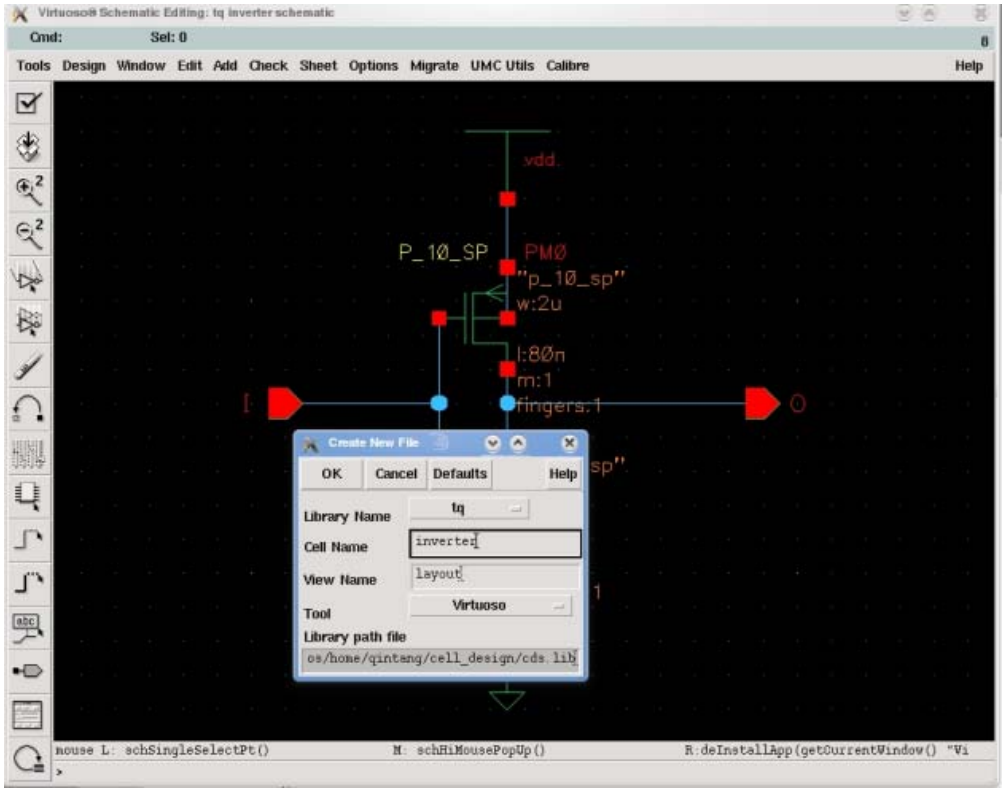

Fig 27. Creating new layout file from schematic

In the **Virtuoso XL Layout** window, select **Design→Gen from source**. The **Layout Generation Options** window will appear (Fig 28). Then, the users need to set up the options in Layout Generation, I/O Pins, and Boundary.

After clicking OK, transistors and I/O pins will appear in the layout view (Fig 29) along with lines showing the circuit connections. Note that if you move any of them, the connecting line follows it (Fig 30).This is very useful for designers because the possibility of incorrect connection is reduced.

NOTE: If you cannot see the device layers (just some black boxes with the device name in them), check the display menu and make sure the configuration is the same as the one you set up in the PMOS layout exercise.

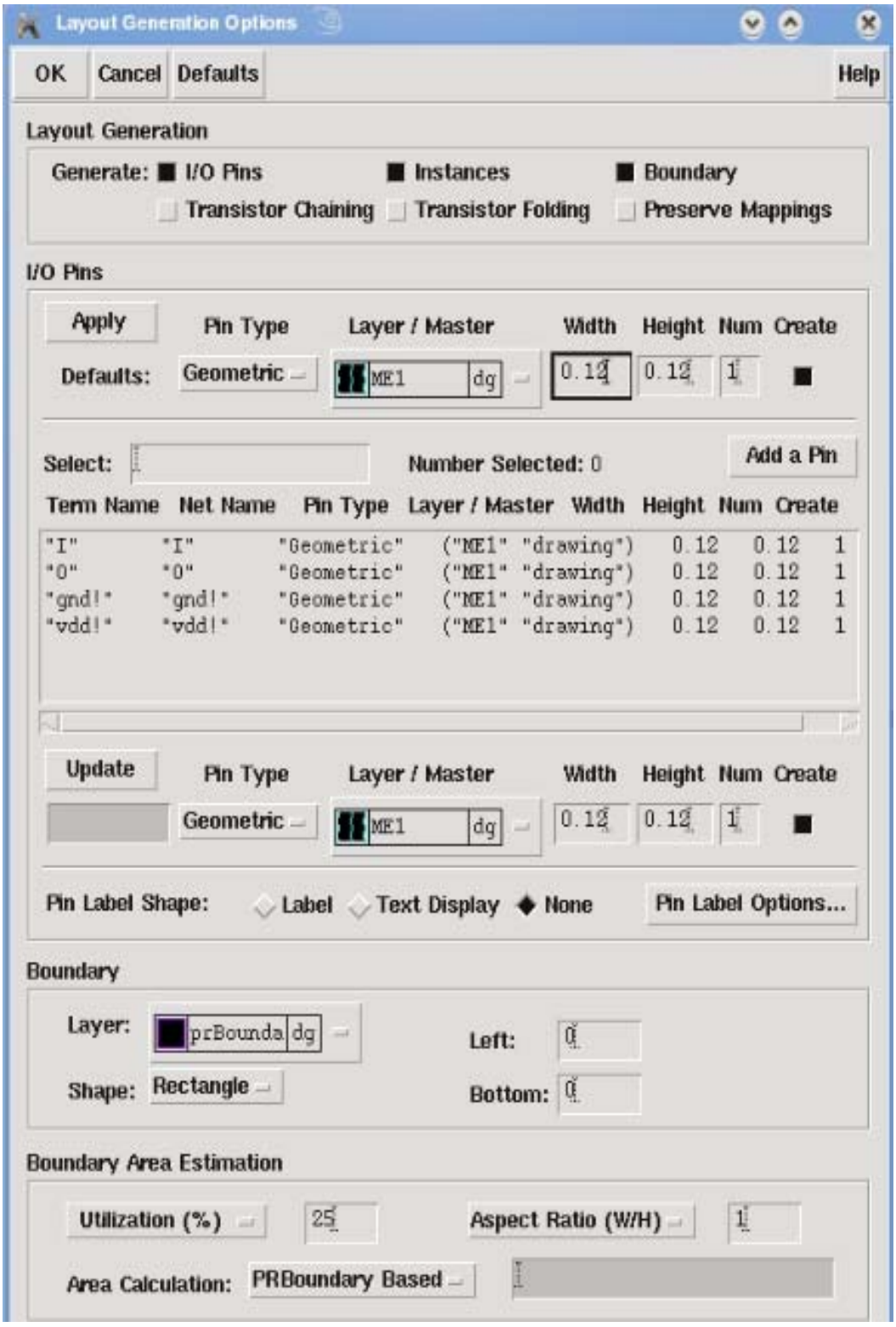

Fig 28. Layout Generation Options window

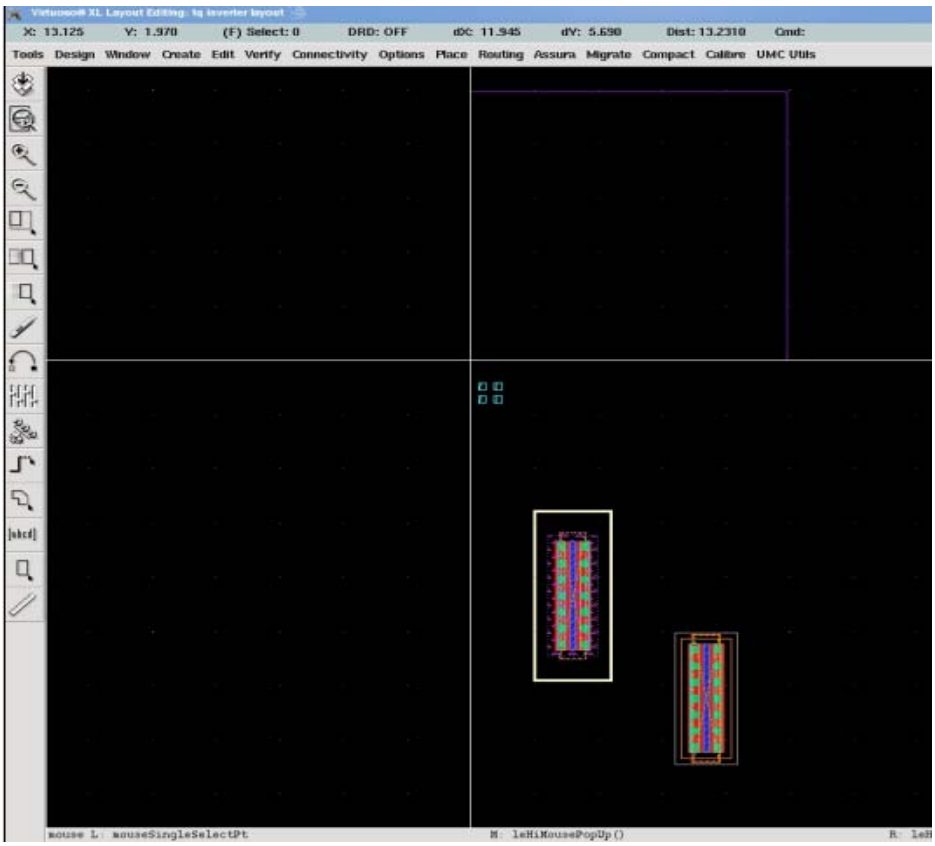

Fig 29. Automatically generated layout

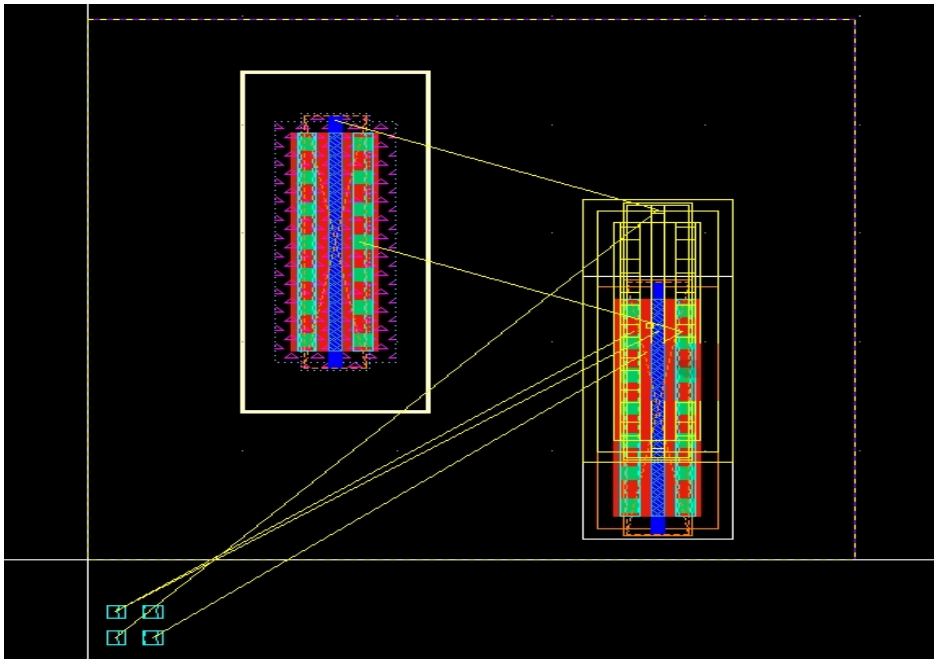

Fig 30. Connections in the layout

The NMOS and PMOS models are placed here automatically but it doesn't mean layout design is completed. Supply voltage (Vdd) and ground (gnd), M1-NWEL and M1-Psub contacts need to be

added and connected. Similarly the source, drain, gate and body pickups should be created and finally, labels need to be added. The complete layout is shown in Fig 31.

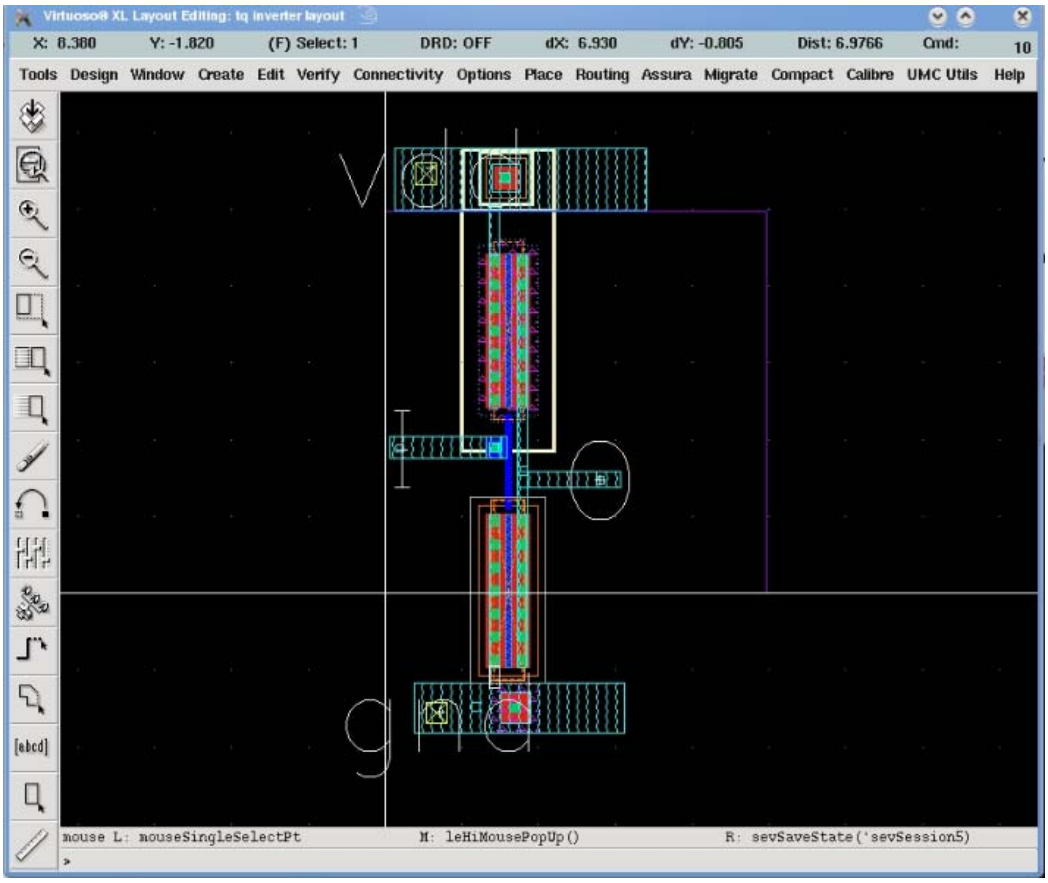

Fig 31. The complete layout

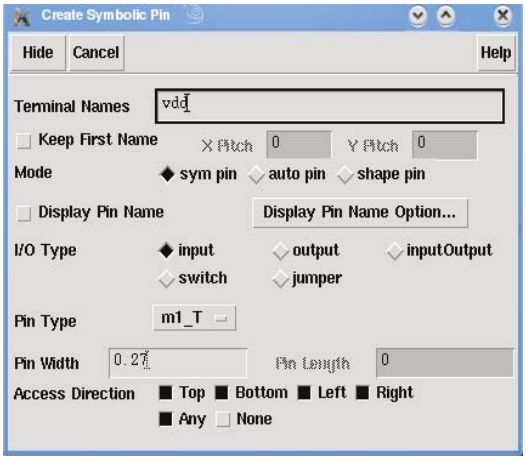

Fig 32. Symbol pin creation

Note:

The labels in layout must be consistent with pin names in the schematic. Select **Create→Pin** in the **Layout Editing** window. **Create Symbol Pin** window will appear (Fig 32). Fill in "Terminal Names", select "I/O Type" and "Pin Width" for different pins. "Pin Type" should be kept as **m1_T** because Vdd, gnd, input I and output O are all connected by **ME1** layer. Click **Hide** then put cursor to the right place and click, the pin name is added successfully.

If layout creation is completed, next step is to run physical verification, in which DRC is the first step. DRC is introduced in detail in previous part. For LVS and PEX, please refer to:

http://www.eda.ncsu.edu/wiki/Tutorial:Layout_Tutorial2

Appendix

The PMOS transistor is made by using the layers as shown in Fig 5. The steps to design this layout are listed below. Considering PMOS layout design is an exercise for you, figures to illustrate each step are not put here, please do the homework by yourself.

1. Choose the **P01** layer, press r to draw a rectangle with the size you want. The minimum width of P01 is 0.08um. The width of P01 determines the channel length.
2. Choose layer **DIFF**, press r to draw active area on the layout. This step defines the active area of the PMOS.
3. Choose the layer **CONT**, Check the minimum distance between P01 and CONT and the minimum DIFF enclosure of the CONT from the Design_rules.ppt, Draw some CONT on the layout. CONT create some holes on the oxide layer for metal contact with the active area, of course all of CONT are in DIFF.
4. Check the minimum P01 overhang of DIFF, use k key to measure the distance. Then press s to stretch P01 layer to modify the poly-gate to fit the requirement. The minimum extension mainly overcomes the misalignment of masks to avoid failure of device
5. Choose **ME1** layer, check minimum width of ME1 and minimum enclosure of CONT from the design rules and then draw two metal1 strips on the layout. The ME1 strips here are used to connect active area of PMOS.
6. Choose the **PPLUS** layer. Check the minimum PPLUS overhang of DIFF, draw the PPLUS implantation mask. The area with PPLUS layer will be implanted to P+ region to ensure ohmic contact between the metal and the substrate.
7. Select **SDSYM** layer, and then draw a rectangle exactly overlapped with channel. I still have no idea about what is SDSYN layer, maybe it is oxide. I didn't find any useful information in data sheet, but in standard library, all kinds of PMOS and NMOS layout have this layer, perhaps it is special requirement of the process.
8. Select **DEVICE** layer to draw device area. Then select **PPLUS** to draw an overlapped area.
9. Select **NWEL** layer. PMOS must be built in Nwell. Check the minimum NWEL enclosure of P+ DIFF (the overlapping area of PPLUS and DIFF). Draw a rectangle in NWEL layer.

Now, click 'check and save' to save your design, and then run Calibre-DRC.

Actually when you design the inverter, you will utilize existing PMOS and NMOS models in the library. But learning how to design PMOS and NMOS transistors by yourself is useful for you to understand fabrication process.