

Write your name and student number on all sheets that you submit

Exam Digital IC Design (ET4293)

Date: Thursday, April 14, 2011 Time: 09.00 am – 12.00 am

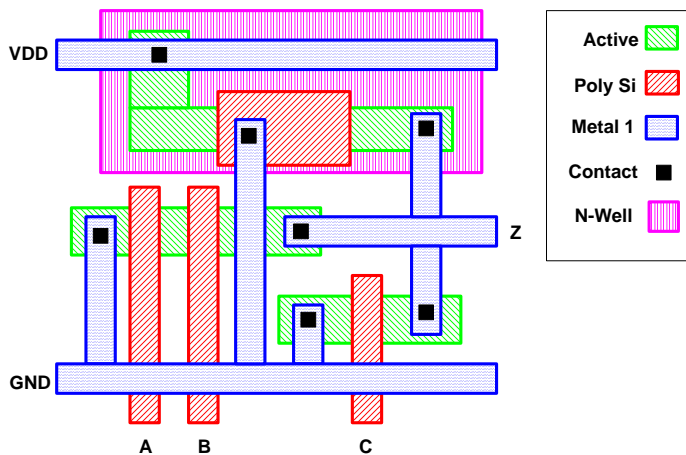
Name:	Student number:	Mark:
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Read first:

- Write your name and student number in the boxes above and on the odd numbered pages.
- This is an open-book exam, you can use the Rabaey book and a printed copy of the lecture slides.
- Whenever technology data is needed and it is not given explicitly, the values from the $0.25\mu\text{m}$ technology from the Rabaey book should be assumed.
- You are allowed to use a non-programmable calculator.
- Circle or cross the right answer of multiple-choice.
- Write your answers on this paper in the reserved spaces. Optionally, you can hand in extra pages. Write your name and student number on these extra pages, and show on the answer sheets that more details are in the separate sheets.
- Logical inverses (Boolean negation) is identified with primes ('). (Sometimes with an overbar.)
- When you need to give an explanation or calculation, be concise but precise. In graphs, always identify and draw/write the relevant values and quantities. Pay attention to the units, and scale factors.
- Each sub question is worth 4 points, for a total of 72 points.

Question 1.

Consider the layout below. Draw its transistor schematic in the box to the right.

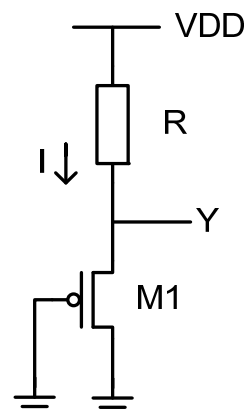


Schematic:

Question 2.

Consider the device configuration to the right. M1 is a minimum size transistor (assume $W/L = 1$). Assume the transistor parameters from the back cover of the book, but assume that $\gamma = 0$ (no body effect) and $\lambda = 0$ (no channel length modulation). Assume a short-channel transistor modelled by the unified model. $V_{DD} = 2V$.

- a.** Write down the equations (and only those) that you need to determine the voltage at node Y. While this does depend on V_Y , do not plug in any values yet. BE COMPLETE and CONSIDER ALL POSSIBLE SOLUTIONS. Determine for each solution when it is valid.



Answer:

b. We would like to place V_Y at 0.8 V. Draw the (approximate) load lines (current I as a function of V_Y) for both the MOS transistor and the resistor in the diagram on the right. Try to have the complete load lines for each region of validity, not just a fraction of them around $V_Y = 0.8$ V. But be careful that the crossing of the load lines of the MOS and of the resistor is in the right part of the curve. You SHOULD identify the relevant/special values on the voltage axis.



c. Determine the value of the resistance R required to have $V_Y = 0.8$ V. Answer below, including calculation.

R =

Calculation:

d. Now assume that the λ -factor (channel length modulation) of the MOS is nonzero, in contrast to what was assumed so far. Determine qualitatively if the voltage at node Y will go up, down or remain unchanged. Explain your answer.

Up

Down

Unchanged

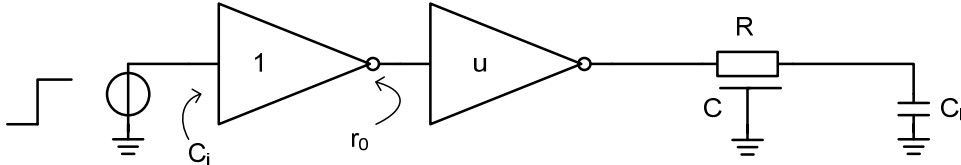
Explanation:

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Question 3.

Consider the circuit below, with a minimum sized inverter driving an u -sized inverter, in turn driving a capacitive load C_L through a wire with resistance R and capacitance C . The minimum size inverter has an input capacitance C_i and an output resistance r_o .



a. What is the propagation delay, t_p , of the above circuit in terms of r_o and the necessary variables given? Use u as a parameter. Give the equivalent RC schematic for explaining your answer.

$t_p =$

Schematic:

b. What value of u minimizes t_p ?

$u =$

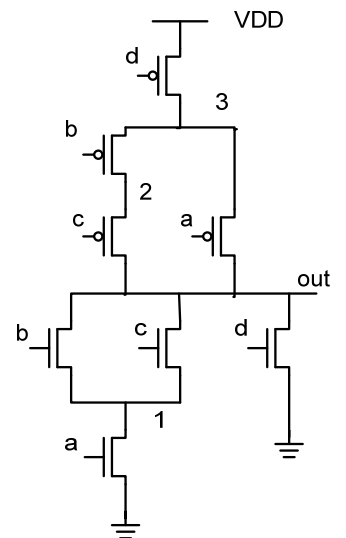
Calculation:

Question 4.

Consider the circuit on the right with internal nodes denoted by numbers 1 ... 3

a. Assuming a load capacitance of 10 fF, determine the transistor sizes for a $t_{pLH} = t_{pHL} = 10\text{ps}$. Assume $L = 1$ and round up each W to integer numbers. Brief calculation below for the **NMOS pull-down transistor for input d only**, write your **answer only for all transistors next to the transistors in the schematic**. You may ignore internal capacitances of this gate.

Calculation for pull-down d :



b. Determine the logical effort of input *b*, assuming a PU/PD ratio of 2.

Logical effort of input <i>b</i> :
Calculation/explanation:

Question 5.

Now consider again the circuit from the previous question, and make the following assumptions:

- The on-resistance of each NMOS and of each PMOS is 10kΩ.
- Each NMOS source or drain contributes 1fF from the node it is connected to, to ground.
- Each PMOS source or drain contributes 3fF from the node it is connected to, to ground.

a. For each of the internal nodes 1, 2 and 3 and the output node *out*, determine the total capacitance to ground. Only answer.

$C_1 =$	$C_2 =$	$C_3 =$	$C_{out} =$
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b. Find the Elmore delay when the inputs *abcd* are initially 1010 and then *a* switches 1→0. Make sure to draw the equivalent circuit diagram you are using, and give your calculation.

Hint: if an intermediate capacitance is already precharged to the correct value, assume that this capacitor contributes nothing to the Elmore delay, and can hence be ignored in the model.

$t_p =$
Schematic and calculation:

Question 6.

a. Again consider the same circuit. Compute the probability of the output *out* being zero if the input probabilities are $P(a=0) = 0.3$, $P(b=0) = 0.4$, $P(c=0) = 0.4$ and $P(d=0) = 0.2$. Assume all inputs to be uncorrelated.

$P(out=0) =$
Explanation/calculation

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b. Now, assume that $P(\text{out}=0) = 0.7$ (this is not necessarily the correct answer to the previous problem). Given a total load capacitance of 25 fF, a supply voltage of 2.5 V and a nominal frequency of 1 GHz (the gate is in the combinational part of a sequential machine, clocked at 1GHz), determine the dynamic power dissipation in W. You may disregard the dissipation internal to this gate (associated with charging and discharging of the internal capacitors).

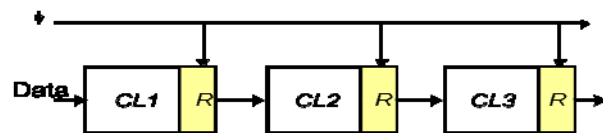
$P_{\text{dyn}} =$

Explanation/calculation

Question 7.

Consider the single-clock phase positive edge triggered pipeline, shown here.

a. What is the constraint that determines the minimum clock period T?



b. Assume that the propagation time of CL1, CL2, and CL3 is 1ns, 2ns, and 3ns, respectively. By tailoring the skews, the clock period can be minimized. Compute the skews (positive or negative) required at each register to minimize T, assuming zero setup time, zero hold time, and zero t_{c-q} .

$\delta_1 =$

$\delta_2 =$

$\delta_3 =$

Explanation/calculation

c. Compute T.

T =

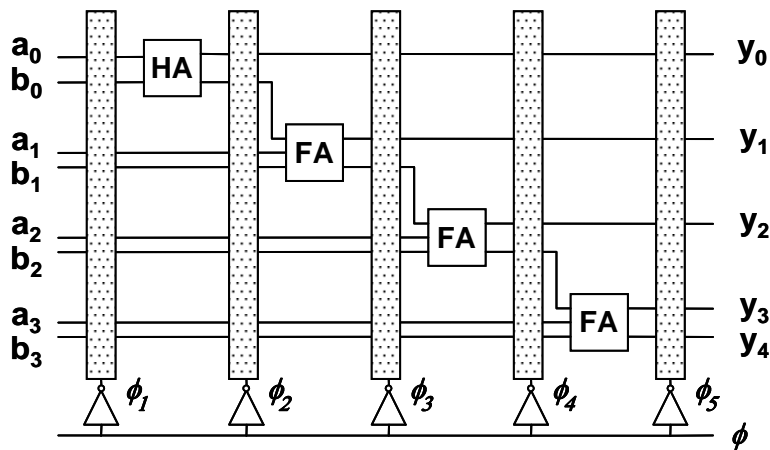
Explanation/calculation

d. Assume $t_{su} = 0.5\text{ns}$, will T need to increase, can it stay unchanged or can it decrease further? How will the latency change, if at all?

T:	Latency:
Explanation/calculation	

Question 8.

Consider the 4-bit adder below. It is pipelined to the bit level, to achieve as high a throughput as possible. The vertical bars denote columns of registers.



Let T_{carry} be the delay of the input of the full adder (or half adder) to the carry output, and T_{sum} the same for the the sum bits. Assume that the delays of the half-adder are equal to those of the full-adders. The maximum clock speed is mainly being determined by:

- A T_{carry}
- B T_{sum}
- C $T_{carry} + T_{sum}$
- D $\text{Max}(T_{carry}, T_{sum})$
- E $\text{Min}(T_{carry}, T_{sum})$

Answer A B C D E (circle answer)
Explanation: