Write your name and student number on all pages that you submit

Exam Digital IC Design (ET4293)

Date: Friday, June 26, 2009 Time: 09.00 am – 12.00 am

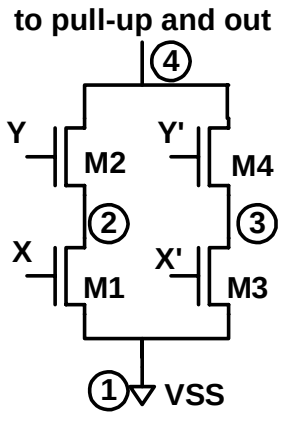
Name:	Student number:	Mark:

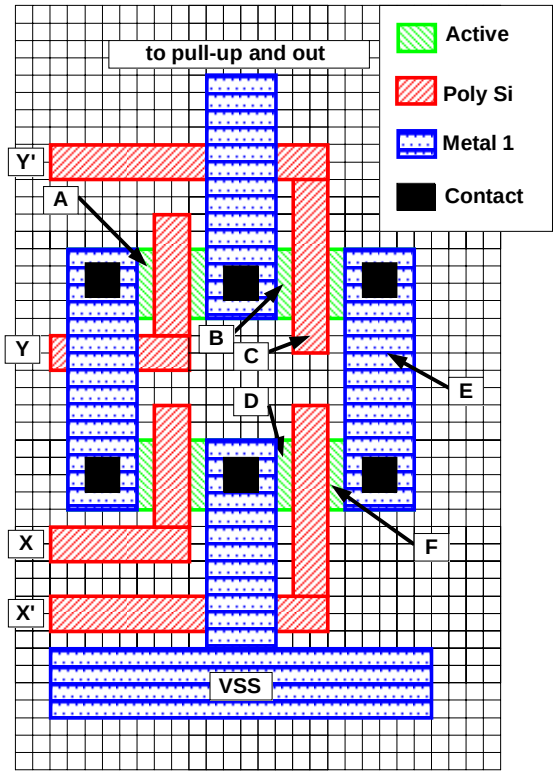
Read first:

- *Write your name and student number in the boxes above and on the odd numbered pages.*
- *This is an open-book exam, you can use the Rabaey book and a printed copy of the lecture slides.*
- *You are allowed to use a calculator.*
- *Circle or cross the right answer of multiple-choice.*
- *Write your answers on this paper in the reserved spaces. Optionally, you can hand in extra pages. Write your name and student number on these extra pages, and show on the answer sheets that more details are in the separate sheets.*
- *Logical inverses (Boolean negation) is identified with primes (‘). (Sometimes with an overbar.)*
- *When you need to give an explanation or calculation, be concise but precise. In graphs, always identify and draw/write the relevant values and quantities. Pay attention to the units, and scale factors.*

Question 1.

The drawing shows a possible layout of the pull-down network of CMOS logic gate, as well as the corresponding schematic. Inversion of logic values is shown wit a prime (‘).





a. Draw the schematic of the corresponding dual pull-up network.

Schematic of pull-up

b. What is the logic function of the gate?

Function:

c. A layout needs to comply with a set of design rules. Explain what kind or rules they are, and explain their purpose.

Explanation:

d. Assume that the output will be loaded with C = 50 fF. Compute the worst-case propagation delay for a high-to-low transition, t_{pHL}. Use the transistor dimensions from the layout. You can use the equivalent on-resistance approximation with R_{eq}; you don't need to apply the current formulas.

t_{pHL} =
Calculation:

e. Which of the transistors M_1 en M_2 in the schematic can experience the body effect?

❑ M_1	❑ M_2
Explanation:	

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f. Discuss the effect of the body effect on the performance of the circuit.

Discussion:

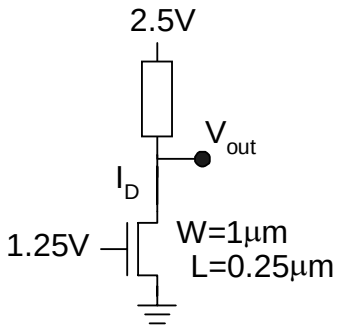
g. Certain areas in the layout correspond to the labeled nodes in the circuit (those identified by a circled number or by the symbols X, X', Y en Y'. The layout regions are identified by arrows and letters A through F. Multiple regions can correspond to the same node, not all nodes in the schematic are necessarily labeled in the layout.

Schematic	Layout
1	
2	
3	
4	

Schematic	Layout
X	
X'	
Y	
Y'	

Question 2.

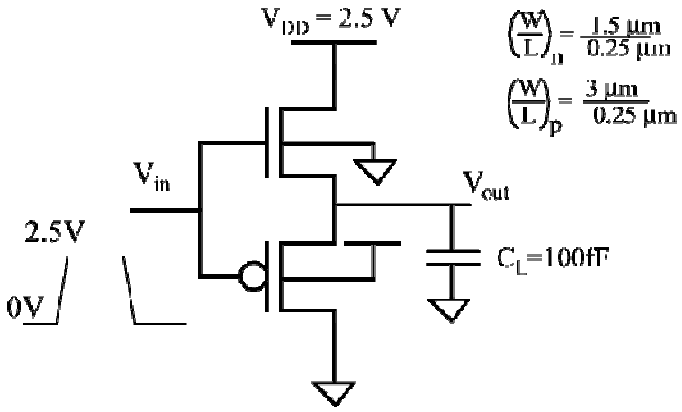
Consider the circuit on the right. Calculate I_D when V_{out} = 0.25 V.
Give the corresponding equation for the region of operation (do not fill in numbers) and the answer.
Assume the parameters from the inside-back cover of Rabaey. Hint: only write the equation and skip the actual calculation if you are on shortage of time.



I_D =
Equation:

Question 3.

Consider the circuit on the right. It can be used as a low-swing driver. Assume the input transition time is 0, the input swing is between 0 and VDD, and take $\phi_f = -0.3V$.



a. Write the equations for V_{OH} and V_{OL} taking into account the body effect in both transistors. First write it using symbols, than fill in numbers. You don't need to solve the equations.

Equation with symbols: V_{OH} =
Equation with values: V_{OH} =
Equation with symbols V_{OL} =
Equation with values: V_{OL} =

b. Assume the output swing is between 0.8 V and 1.7 V. To estimate the t_{pHL}, you want to compute the current delivered by the PMOS. What is (are) the operating region(s) of the PMOS transistor? Clearly give the ranges of V_{out} for each operating region that you find.

Operating regions and voltage ranges:

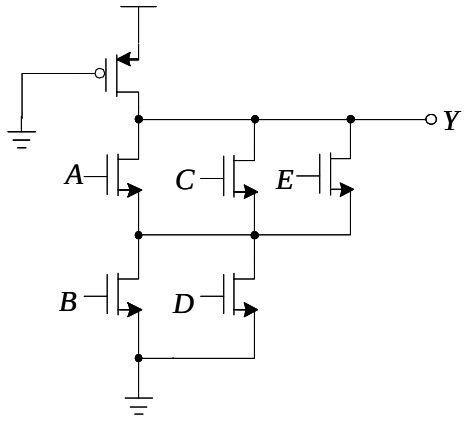
c. Assume that the average pull-down current over the full output swing is 400 μA. Calculate $t_{pHL.}$

t_{pHL} =
Calculation:

Name:	Student number:

Question 4.

Consider the circuit on the right. All NMOS transistors have the W/L ratio of 3. Use the R_{eq} data from the Rabaey tables. VDD is 2.5 V.



a. What is the logic function of the output Y?

Y =

b. If the input is 10011, calculate the effective pull-down resistance. Only answer, no calculation.

$\mathbf{R_{pd}}$ **=**

c. Consider 2 scenarios. In scenario A, the input goes from 01000 to 11000. In scenario B, the input goes from 10000 to 11000. Which scenario is faster (which as the lowest T_{pHL})? Circle the right answer, and explain.

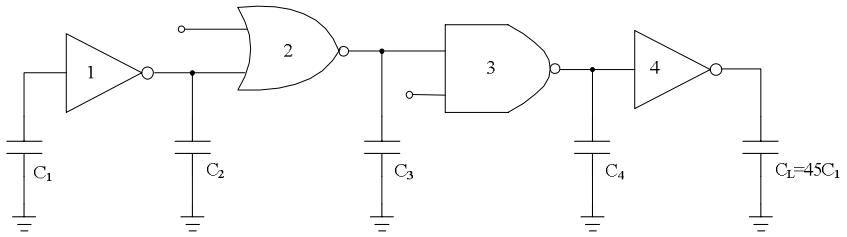
Scenario A is faster	Scenario B is faster	Both are equally fast	Cannot determine
Explain:			

Question 5.

a. The logical effort of an inverter is 1. Determine the logical effort of a NOR-2 gate which is used as an inverter (2 inputs wired together).

g =
Explanation/calculation:

Question 6.



a. Calculate the optimum sizing for the logic circuit shown above. C_i denotes the gate capacitance of gate *i*. The size of gate *i* will be denoted as S_i. The load capacitance C_L is 45 times the gate capacitance of the first inverter C_1. Determine the sizes S_2-S_4 of gates 2-4 respectively (in multiples of the size of gate 1) that minimize the path delay. Assume $\gamma = 1$.

S_2 =	S_3 =	S_4 =
Calculation:		

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Question 7.

a. Consider a possible implementation for a 2-phase non-overlapping clock generator as shown on the right. Draw the waveforms for CLK_1 and CLK_2 below, given the waveform of CLK_0. The clock period is 20τ, as shown on the horizontal axis of the waveform. The propagation delays of the inverter, buffer and NAND gates are τ, τ, and 2τ respectively, as indicated in the figure. Assume all rise and fall times are 0 (infinite slopes).