Write your name and student number on all pages that you submit

Exam Digital IC Design (ET4293)

Date: Thursday, April 2, 2009 Time: 09.00 am – 12.00 am

Name: ANSWERS	Student number:	Mark:

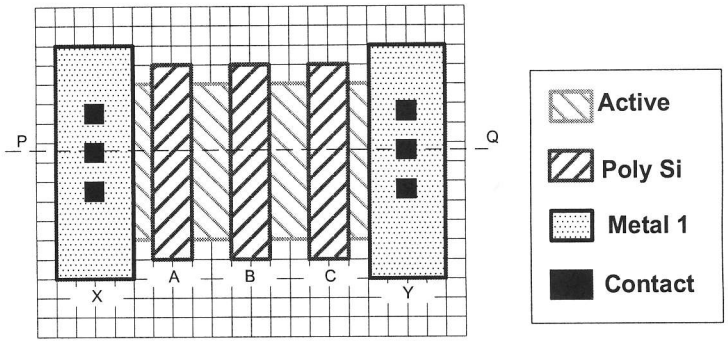
Read first:

- *Write your name and student number in the boxes above and on the odd numbered pages.*
- *This is an open-book exam, you can use the Rabaey book and a printed copy of the lecture slides.*
- *You are allowed to use a calculator.*
- *Circle or cross the right answer of multiple-choice.*
- *Write your answers on this paper in the reserved spaces. Optionally, you can hand in extra pages. Write your name and student number on these extra pages, and show on the answer sheets that more details are in the separate sheets.*
- *Logical inverses (Boolean negation) is identified with primes (').* (Sometimes with an overbar.)
- *When you need to give an explanation or calculation, be concise but precise. In graphs, always identify and draw/write the relevant values and quantities. Pay attention to the units, and scale factors.*

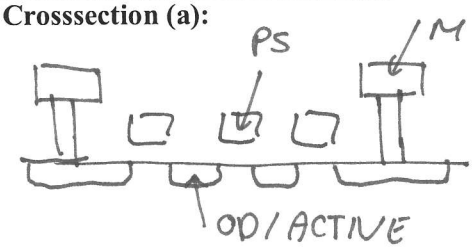
Question 1.

Consider the layout on the right.
a. Draw the cross-section along the line P-Q. Clearly identify the material types.

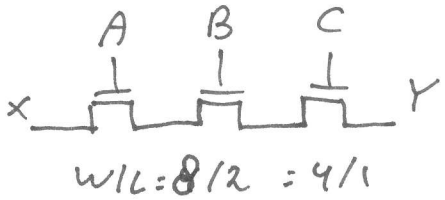
b. Draw the corresponding circuit diagram (schematic). Clearly identify which nodes in the schematic correspond to the letters X, Y, A, B and C in the layout. Also identify the W/L ratios of the transistors in the schematic.



Crosssection (a):

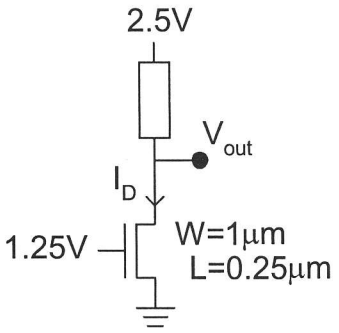


Schematic (b):



Question 2.

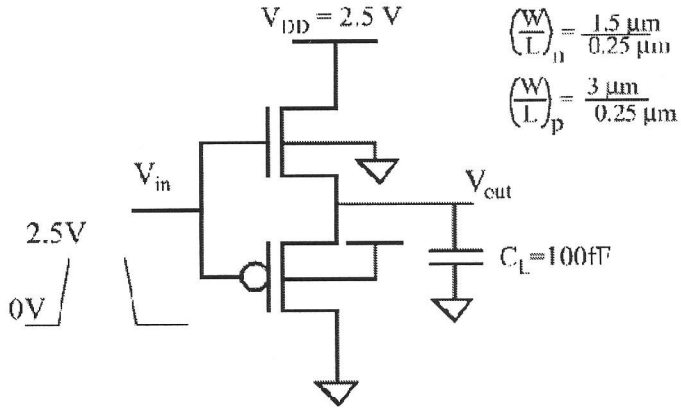
Consider the circuit on the right. Calculate I_D when V_{out} = 1.25 V.
Give the corresponding equation for the region of operation (do not fill in numbers) and the answer.
Assume the parameters from the inside-back cover of Rabaey.
Hint: only write the equation and skip the actual calculation if you are on shortage of time.



I_D = 157.3μA
Equation: $I_D = k'_n \frac{W}{L}\left((V_{GS}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)(1+\lambda V_{DS})$ $= 115.10^{-6} \cdot 4\left((1.25-0.43)0.63 - \frac{(0.63)^2}{2}\right)(1+0.06\times 1.25) = 157.3\mu A$

Question 3.

Consider the circuit on the right. It can be used as a low-swing driver. Assume the input transition time is 0, and take $\phi_f = -0.3V$.



a. Write the equations for V_{OH} and V_{OL} taking into account the body effect in both transistors. First write it using symbols, than fill in numbers. You don't need to solve the equations.

Equation with symbols:	$V_{OH} = V_{DD} - V_{Tn}$ $V_{Tn} = V_{T0} + \gamma_n\left(\sqrt{2\lvert\phi_F\rvert + V_{OH}} - \sqrt{2\lvert\phi_F\rvert}\right)$
Equation with values:	V_{OH} =
Equation with symbols	$V_{OL} = \lvert V_{Tp}\rvert$ $V_{Tp} = V_{Tp0} + \gamma_p\left(\sqrt{2\lvert\phi_F\rvert + V_{DD} - V_{OL}} - \sqrt{2\lvert\phi_f\rvert}\right)$
Equation with values:	V_{OL} =

b. Assume the output swing is between 0.8 V and 1.7 V. To estimate the t_{plLH}, you want to compute the current delivered by the NMOS. What is (are) the operating region(s) of the NMOS transistor? Clearly give the ranges of V_{out} for each operating region that you find.

Operating regions and voltage ranges:

Can't be linear, since $V_{GD} = 0$ when V_{in} input high.
Thus: normal saturation or velocity saturation.
Since $V_{DD} - V_{DSAT} = 2.5 - 0.63 = 1.87 > V_{out\,max}$
we have velocity saturation.

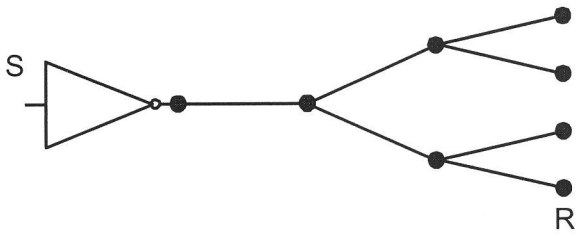
c. Assume that the average pull-up current over the full output swing is 400 μA. Calculate t_{pLH}..

t_{pLH} = 225ps
Calculation: $400\mu A \times t_{PLH} = 100fF \cdot (1.7-0.8) \Rightarrow t_{PLH} = 225ps$

Name:	Student number:

Question 4.

The drawing on the right schematically shows a clock-distribution network. Each one of the 7 segments (each line segment in the schematic) is 1 mm long and 1 μm wide, and is implemented in Metal 1. Each endpoint such as R is loaded with a capacitance of 200fF. Use the technology data from the inside-back cover of the Rabaey book.



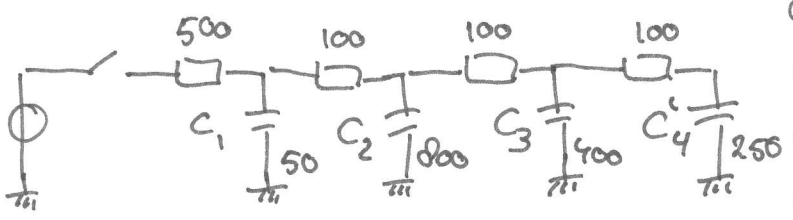
a. When the total capacitance of all segments together amounts to 1pF (which is not the correct answer to the next question), calculate the average current that the driver (the inverter) should deliver for a 50% delay of 1ns. For this question, please disregard the resistance of the wires. Assume V_{DD} = 2.5V.

I_{avg} = 2.25mA (don't forget scaling factor)
Calculation: because $t_{50\%}$ ↓ $C_{total} = 1pF + 4 \times 0.2pF = 1.8pF$ $I_{AVG} = \frac{C\Delta V}{t} = \frac{1.8.10^{-12}\,pF \times 1.25\,V}{1.10^{-9}\,s} = 2.25mA$

b. Calculate the resistance and capacitance of *one* segment (rounding/approximation errors of about 10% are allowed – it is important to show a correct calculation procedure).

R = 50Ω	C = 110fF
Calculation: $R = \frac{1000}{1} \times 0.05 = 50\Omega$ $C = 1000 \times 30 + 2000 \times 40 = 0.11pF$ ↑ C_{area} ↑ $2 \times L$ ↑ C_{fringe}	

c. Now, assume that each segment has a resistance of 100 Ω and a capacitance of 100 fF (these are not the correct answers to the previous question). Also assume that the output impedance of the driver is 500 Ω, but you may ignore the output capacitance of the driver. Consider the Elmore delay formula for the delay from S to R. Draw a simple RC circuit for modeling the Elmore delay, and give the values of each R and C in the schematic. Also include the 200fF load cap at each terminal.



$C_1 = 0.5 \times 100$
$C_2 = 4 \times 100 + 2 \times 200$
$C_3 = 2 \times 100 + 1 \times 200$
$C_4 = 0.5 \times 100 + 1 \times 200$
All C in fF

d. Calculate the Elmore delay for the circuit in your answer to question **c.**.

$T_{D,R}$ = 985ps

Calculation

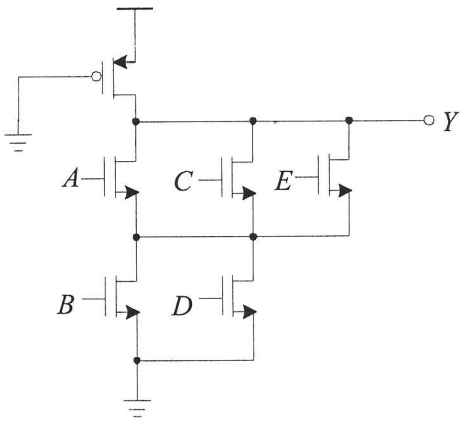
$500 \times 50 + 600 \times 800 + 700 \times 400 + 800 \times 250$

$= 985000\ \Omega . 10^{-15} F$

$= 985ps.$

Question 5.

Consider the circuit on the right. All NMOS transistors have the W/L ratio of 3. Assume the on-resistance for NMOS device with W/L of 1 is R_{on}.



a. What is the logic function of the output Y?

Y = $(A+C+E)(B+D)$

b.Give the input values (logic values, either 1 or 0) for the best-case and worst case pull-down resistance.

ABCDE = 11111 (best case) x g x g x worst case only one x and only one g = 1, others 0

c. If the input is 11000, calculate the effective pull-down resistance. Only answer, no calculation.

R_{pd} = $\frac{2}{3} R_{on}$

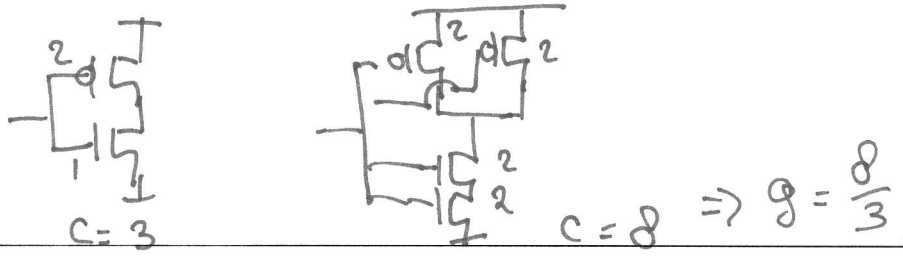
Question 6.

a. The logical effort of an inverter is 1. Determine the logical effort of a NAND-2 gate which is used as an inverter (2 inputs wired together).

g = $8/3$

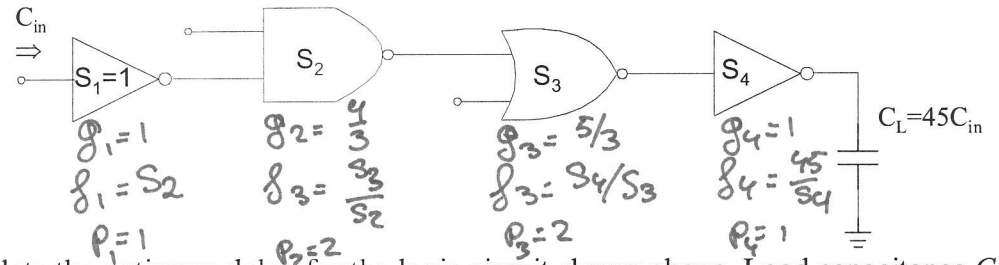
Explanation/calculation:

Ratio of input cap for same drive strength (assume $P_0/P_{0,ref} = 2$)



Name:	Student number:

Question 7.



a. Calculate the optimum delay for the logic circuit shown above. Load capacitance C_L is 45 times the gate capacitance of the first inverter *Cin*. Determine the sizes S_2-S_4 and the minimum delay expressed in term of t_{p0} (intrinsic delay). Assume $\gamma = 1$.

$S_2 = 3.16$	$S_3 = 7.5$	$S_4 = 14.23$

Calculation: $F = \Pi f_i = 45$ $G = \Pi g_i = \frac{20}{9}$ $H = GF = 100$

$h_{opt} = (100)^{1/4} = \sqrt{10}$

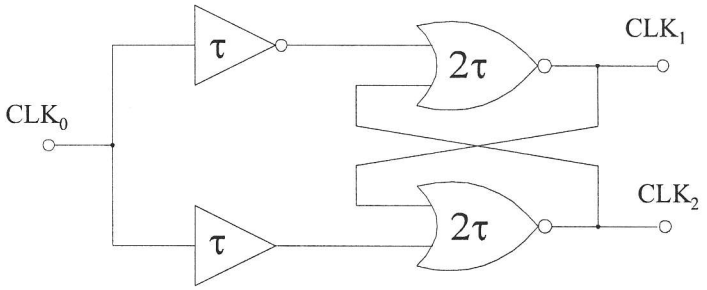
$g_1 f_1 = S_2 = \sqrt{10} = 3.16$

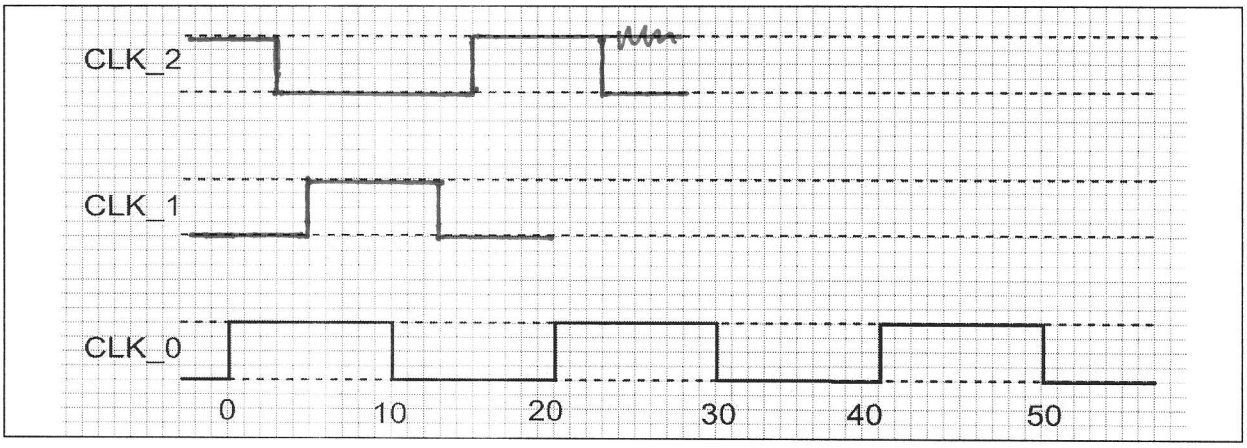
$g_2 f_2 = \frac{4}{3}\frac{S_3}{S_2} = \sqrt{10} \Rightarrow S_3 = 7.5$

$g_3 f_3 = \frac{5}{3} S_4/S_3 = \sqrt{10} \Rightarrow S_4 = 4.5\sqrt{10} = 14.23$

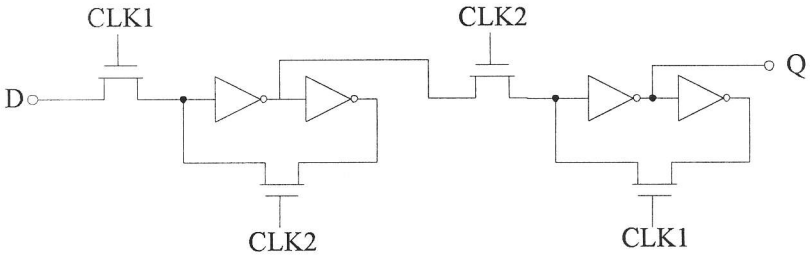
Question 8.

a. Consider a possible implementation for a 2-phase non-overlapping clock generator as shown on the right. Draw the waveforms for CLK_1 and CLK_2 below, given the waveform of CLK_0. The clock period is 20τ, as shown on the horizontal axis of the waveform.

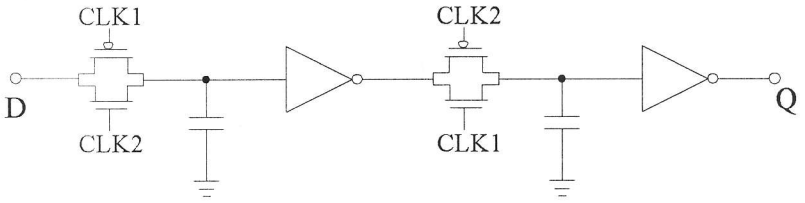




b. Now consider the 2 types of registers as shown on the right. Determine if the waveforms above are suitable to drive each of these two styles of registers. Explain your answer if it is negative.



a: Master-slave register based on NMOS-only pass transistors



b: Dynamic edge-triggered register

Register a: Yes/No	**Register b:** Yes/No
Explanation: Direct path in (b) during 0-0 overlap (a) works because of data retention on (parasitic) C	