# A 2.1 µW/Channel Current-Mode Integrated Neural Recording Interface

Amir Zjajo, Rene van Leuken

***Abstract*—In this paper, we present a neural recording interface circuit for biomedical implantable devices, which includes low-noise signal amplification, band-pass filtering, and current-mode successive approximation A/D signal conversion. The integrated interface circuit is realized in a 65 nm CMOS technology, and consumes less than 2.1 µW/channel of which A/D converter consumes 367 nW, corresponding to a figure of merit of 14 fJ/conv.-step, while operating from a 1 V supply.**

## I. Introduction

Bio-electronic neural interfaces enable the interaction with neural cells by recording, to facilitate early diagnosis and predict intended behavior before undertaking any preventive or corrective actions, or by stimulation, to prevent the onset of detrimental neural activity such as that resulting in tremor. Multi-channel neural interfaces allow for spatial neural recording and stimulation at multiple sites [1]-[4]. To evade the risk of infection, these systems are implanted under the skin, while the recorded neural signals and the power required for the implant operation is transmitted wirelessly. The maximum number of channels is constrained with noise, area, bandwidth, power, which has to be supplied to the implant externally, thermal dissipation i.e. to avoid necrosis of the tissues, and the scalability and expandability of the recording system. Very frequently an electrode records the action potentials from multiple surrounding neurons. Subsequently, the ability to differentiate spikes from noise is governed by, both, the discrepancies between the noise-free spikes from each neuron, and the signal-to-noise level (SNR) of the recording interface. After the waveform alignment, a feature extraction step characterizes detected spikes and represent each detected spike in a reduced dimensional space. The feature extraction and spike classification significantly reduce the data requirements prior to data transmission (in multi-channel systems, the raw data rate is substantially higher than the limited bandwidth of the wireless telemetry [5]). A 128-channel, 10-bit-precise digitization of neural waveforms sampled at 40 kHz generates ~ 51 $Mbs^{-1}$ of data; the power costs in signal conditioning, quantization and wireless communication all scale with the data rate.

In this paper, we introduce a novel, low-power neural recording interface system with capacitive-feedback low-noise amplifier, capacitive-attenuation band-pass filter, and current-mode A/D converter (ADC). The capacitive-feedback amplifier offers low-offset and low-distortion solution with optimal power-noise trade-off.

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A. Zjajo and R. van Leuken are with Circuits and Systems Group, Delft University of Technology, Mekelweg 4, 2628 CD, Delft, The Netherlands; (e-mail: amir.zjajo@ieee.org).

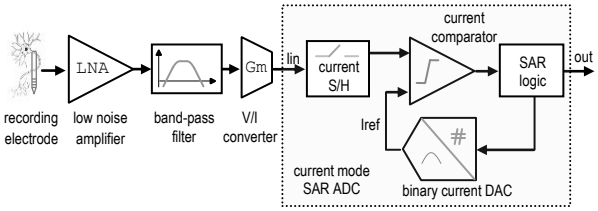



Figure 1: Functional overview of the system level design of the proposed current-mode front-end neural recording interface (for simplicity, only one channel shown).

Similarly, the capacitive-attenuation band-pass filter provides wide tuning range and low-power realization, while allowing simple extension of the transconductors linear range, and consequently, ensuring low harmonic distortion. The current-mode converters offer high resource efficiency in terms of power and area [6]-[9]. In contrast to voltage-mode, charge redistribution SAR A/D converters, corresponding current mode circuit have several intrinsic advantages, including tunable input impedances, wide bandwidth, and low supply voltage requirement. Additionally, only MOSFET devices are required for logical and numerical operation limiting the area requirements. The implementation results in a 65 nm CMOS technology show that a significant gain on throughput, resource usage and power reduction (less than 2.1 µW per recording channel of which A/D converter consumes 367 nW, corresponding to a figure of merit of 14 fJ/conv.-step) can be obtained for large-scale neural spike data, allowing for an efficient and easily-scalable system.

## II. Circuit Implementation

### A. Architectural Overview

With an increase in the range of applications and their functionalities, neuroprosthetic devices are progressing towards a closed-loop control system [10] with front-end neural recording interface, and a back-end neural-signal processing. The block diagram of a *N*-channel neural recording system is illustrated in Figure 1. The data attained by the recording electrodes is conditioned with analog circuits. The small amplitude of neural signals and the high impedance of the electrode-tissue interface necessitate a low-noise amplification (LNA) and band-pass filtering before the voltage signals are transformed into current by the V/I converter, and digitized by a current mode SAR A/D converter. The output digital code is generated by comparing the input current offered through current sample-and-hold circuit (S/H), with a reference current provided by binary current D/A converter (DAC). The current comparison necessitates only injecting two currents into a single node and using the current, which flows out of the node, as the algebraic difference of the two input currents.

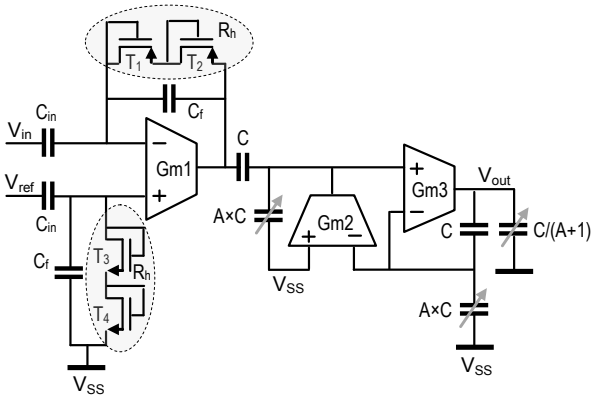



Figure 2: Schematic of the low noise neural amplifier, and the capacitive attenuation band-pass filter.

The current comparison is performed sequentially for each bit in the selected range, adjusting the reference current generated by a current mode D/A converter closer to the input signal. The input dynamic range of the D/A converter is controlled by biasing current. As a consequence, the power consumed by the D/A converter is directly comparable to the signal level, which is highly beneficial for the neural interface circuits containing low energy neural signals. The SAR A/D converter output signal is further processed in a back-end signal processing unit, which provides additional filtering and executes a spike detection. The relevant information is then transmitted to a receiver, or used for stimulation in a closed-loop framework.

### *B. Signal Conditioning Circuit*

The neural spikes, ranging from 10 μV to 500 μV (and containing data of up to ~20 kHz), are amplified with low noise amplifier (LNA) illustrated in Figure 2. The transconductance ($G_m$) (i.e. V/I converter) based amplifier has a capacitive feedback configuration, which is adapted from [11] with minor modifications. Two identical diode-connected transistors $T_{1\text{-}2}$ and $T_{3\text{-}4}$ act as a high ohmic resistors $R_h$, and adjust the high-pass cut-off of the LNA at $(2\pi R_h C_f)^{-1}$ blocking the *dc* offset generated by the electrode-tissue interface and local field potentials. The mid-band gain $A_{mb}$ is set by $C_{in}/C_f$ with the low-pass cut-off frequency at $\sim g_{m,in}/(2\pi C_L)$, where $C_L$ is the effective load capacitance of the amplifier, and $g_{m,in}$ is the transconductance of the input transistors. Implemented $G_{m1}$ folded cascode circuit is illustrated in Figure 3a).

The topology is based on [12], where current splitting technique to enhance the drain resistance of both input and bottom transistors without any additional cascading, is combined with the output-current scaling [13] to lower the OTA noise. The folded cascode $G_{m1}$ circuit realize a wide input common-mode range, and a relatively large open-loop gain within the single stage. An input-referred electronic noise of an integrated front-end negative-feedback amplifier needs to be smaller than the total input noise from the neural electrode (10~20 $\mu V_{rms}$ [14]). The input-referred noise of the $G_{m1}$ circuit is reduced by maximizing input pair $g_m$, the use of cascaded resistive loading (rather than current-source loads), and minimizing $g_m$ of the current sources (and mirrors). The bias current of the $G_{m1}$ can be varied to adapt its noise per unit bandwidth. The transistors of the output stage have two constrains: to increase the output resistance of the cascade and allow sufficient *dc* gain, the $g_m$ of the cascading transistors $T_{9,}T_{12}$ must be high enough. Secondly, to reduce the extra noise contribution of the output stage, the saturation voltage of the active loads $T_{5\text{-}8}$ and $T_{13\text{-}16}$ must be maximized. By increasing the size of the cascading transistors above the active loads, the $g_m$ of the cascading transistors is maximized, and consequently, the *dc* gain increased. Simultaneously, their saturation voltage is reduced (i.e. allowing for a larger saturation voltage for the active loads), without exceeding the voltage headroom.

To keep the overall bandwidth constant, when the bias current of the gain stage is varied, a band-pass filter [15] (Figure 2) is added to the output of the LNA. High gain of the LNA reduces noise requirements of this bandwidth-limiting circuit. The total integrated output voltage noise of the filter depends on the linear range of the transconductors $G_{m2}$ and $G_{m3}$ (Figure 3b), the ratio of the attenuator capacitances $A$ and the unit capacitance $C$. The linear range is effectively improved by attenuating the input. In the high-pass stage, the signal is attenuated with $A$+1, and the full capacitance of $(A+1)C$ is then utilized for filtering with $G_{m2}$. In the low-pass stage, signals in the pass-band are amplified with $A$+1. To increase the filtering capacitance, additional capacitance $C/(A+1)$ is placed in parallel with the attenuating capacitances. Dynamically biased $G_{m3}$ cell illustrated in Figure 3c) offers highly linear voltage to current conversion. The cross-coupled transistors $T_{3\text{-}4}$ and $T_{13\text{-}14}$ ensure the rail-to-rail differential-input swing and linear output current with a dynamic adjustment of the input window.

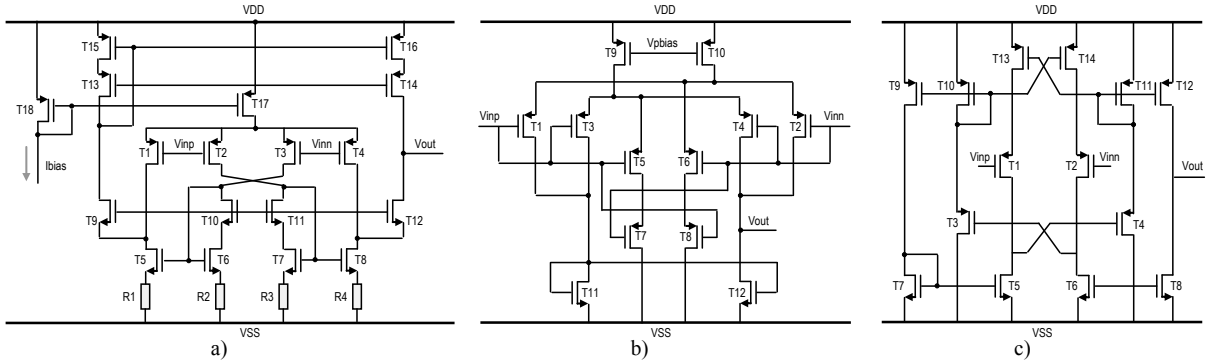



Figure 3: a) Folded cascode LNA $G_{m1}$ circuit, b) band-pass filter $G_{m2}$ cell, c) band-pass filter $G_{m3}$ cell

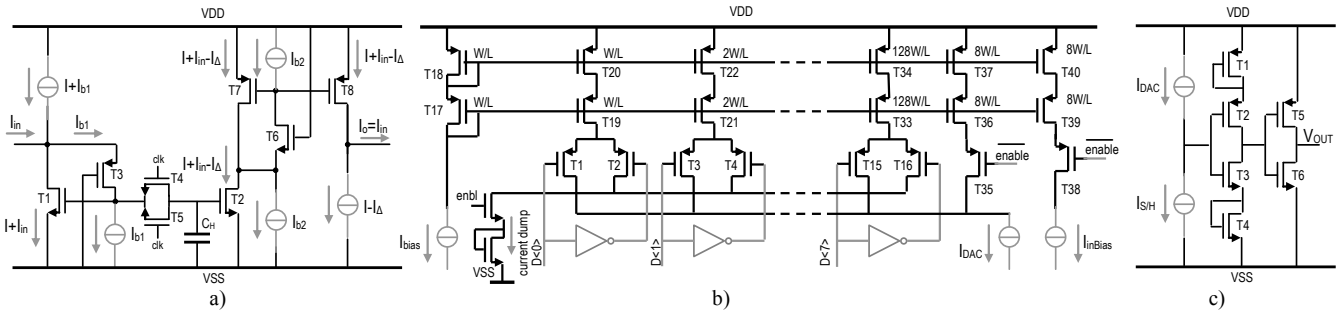



Figure 4: a) Schematic of current-mode S/H circuit, b) current-mode D/A converter, c) schematic of the inverter cascade current-mode comparator circuit.

### C. *Current-Mode Signal Quantization Circuit*

A S/H circuit capture the input signal at the sampling instants and subsequently hold the signal value, which is then further processed in a current based binary search algorithm SAR loop. The schematic of the implemented circuit is illustrated in Figure 4a). The circuit is (pseudo) differential, and only a single-ended version is shown. A sample-and-hold operation is completed with analog switch formed by transmission gate $T_{4\text{-}5}$ and hold capacitor $C_H$. In sample mode, switch $T_{4\text{-}5}$ is turned on, and the gates of the current-mirror circuit transistors $T_1$ and $T_2$ become connected. Accurate current-mirroring operation is performed if the drain voltages of both transistors are equal. However, the accuracy of the current-mirror formed by transistors $T_1$ and $T_2$ is limited, generating a signal-dependent current conversion error $I_\Delta$. Consequently, two operational amplifiers are added [16], one at the input terminal (formed by transistor $T_3$ and current source $I_{b1}$) and one at the output terminal (formed by transistor $T_6$ and current source $I_{b2}$) to keep the input and the output terminal voltages of a current mirror circuit constant.

The current mode D/A converter circuit illustrated in Figure 4b) consists of a current switching circuit of differential pairs ($T_{1\text{-}16}$) controlled by the binary bits, and a current replication circuit to generate weighted currents using cascoded current mirrors ($T_{17\text{-}34}$). The cascoded current sources are sized up consistent with the bit weight, and biased with identical bias voltages. This compact implementation is limited only by the steepness of the data waveforms carrying the bits, and at nA bias levels, by transistor mismatch limiting the linearity and restricting the maximum resolution [17]. To achieve an 10-bit resolution, calibration as in [6] is employed. The converter utilizes a synchronous SAR logic consisting of a cascade multiple input, *n* bit shift register to generate digital output code, and the switch control signals for the D/A converter. During conversion process, the successive approximation algorithm evaluates each bit and the state of the others, and subsequently, decides either to hold its value or to take the value of the comparator [18]. The selection depends on the state of the register itself and the state of the following registers states. As a result, switching power consumed is low, and the leakage power dominates the total power. To reduce the leakage currents the gate transistors are replaced with stacked pairs [19].

The current difference between the sample and hold output current $I_{S/H}$ and the D/A converter output current $I_{DAC}$ is integrated by the input gate capacitance of the inverter cascade current comparator $T_{1\text{-}4}$ illustrated in Figure 4c). The first inverter operates as an integrating current-to-voltage converter, while the second inverter $T_{5\text{-}6}$ changes the sign of the first inverter output voltage to the equivalent of the input current. The integrating nature of the comparator ensures that no inherent *dc* offset is present in the comparator, and provides a small and effective current-to-voltage conversion.

## III. Experimental Results

Design simulations on the transistor level were performed at body temperature (37 ºC) on Cadence Virtuoso using industrial hardware-calibrated TSMC 65nm CMOS technology. The analog circuits operate with a 1 V supply, while the digital blocks operate at near-threshold from a 400 mV supply. The test dataset (Figure 5) is based on recordings from the human neocortex and basal ganglia. The fully differential low-noise amplifier achieves 55 dB closed loop gain, and occupies an area of 0.04 $mm^2$. Input referred noise is 3.1 $\mu V_{rms}$ over 0.1-20 kHz. THD is below 1% for typical extracellular neural signals (smaller than 10 mV peak-to-peak). The common-mode rejection ratio (CMRR), and the power-supply rejection ratio (PSRR) exceeds 75 dB. The capacitive-attenuation band-pass filter with first-order slopes achieves 65 dB dynamic range, 210 $mV_{rms}$ at 2% THD, and 140 $\mu V_{rms}$ total integrated output noise. Spectral signature of the neural interface is illustrated in Figure 6a). As shown in Figure 6b) and Figure 6c), SNDR, SFDR and THD remain constant at different input and sampling frequencies, respectively. Variation across slow-slow and fast-fast corner is ± 0.2 ENOB. The DNL/INL is ±0.2/0.3 LSB, respectively.

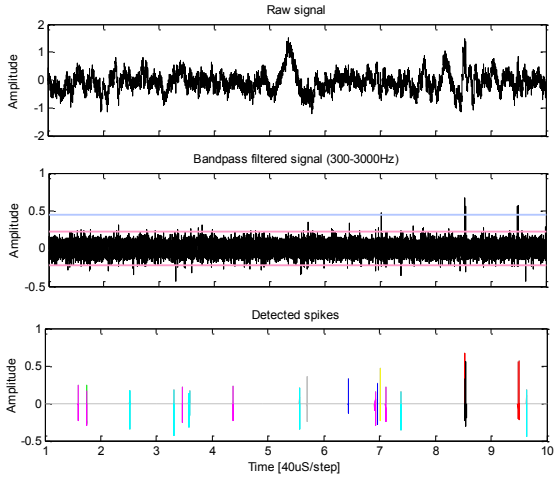
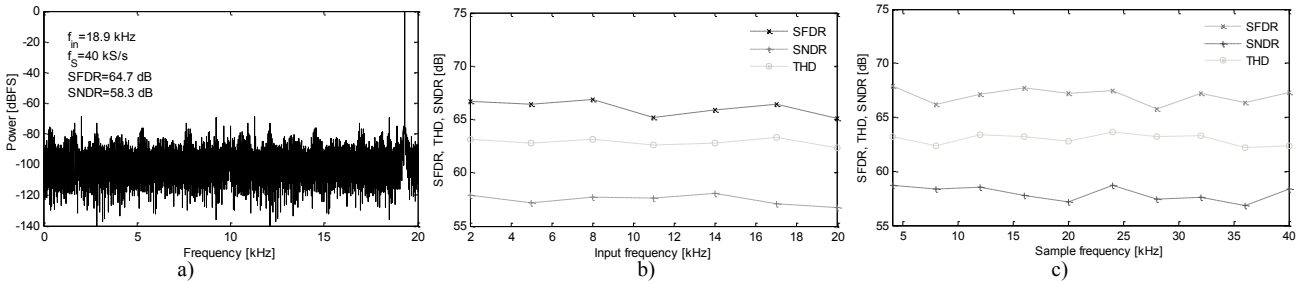



Figure 5: Test data set, the *y* axis is arbitrary; a) top: raw signal after amplification, not corrected for gain, b) bandpass filtered signal, and c) detected spikes; a) and b) not on the same time-scale.




a) b) c)

Figure 6: Spectral signature of the neural interface, b) SFDR, SNDR and THD vs. input frequency with $f_S$=20 kHz, c) SFDR, SNDR and THD vs. sampling frequency with $f_{in}$=1 kHz.

Low noise amplifier consumes 1.15 µW, and band-pass filter 390 nW of power, while SAR A/D converter consumes 367 nW (sample and hold 117 nW, comparator 37 nW, D/A converter 149 nW and logic 64 nW). The specifications of the current mode SAR A/D converter is compared with the previous art in Table I, where the figure of merit (FoM) is calculated according to FoM=$P/(2f_{in}\times 2^{ENOB})$ [J/conversion-step] [20]. In Table II, we compare the state of the art neural recording systems to this work.

| *ADC* | *[6]** | *[7]** | *[8]** | *[9]** | ***[this work]**** |
|---|---|---|---|---|---|
| *Technology* | *0.18* | *0.18* | *0.18* | *0.13* | *0.065* |
| *Resolution* | *8* | *6* | *8* | *8* | *10* |
| *$V_{DD}$ [V]* | *1.2* | *0.65* | *0.55* | *1* | *1* |
| *$f_S$ [kS/s]* | *16* | *120* | *250* | *1* | *40* |
| *THD [dB]* | *-* | *-* | *-* | *47.5* | *63.4* |
| *FoM [J/con-s]* | *132f* | *8p* | *9f* | *657f* | *14f* |
| *Power [W]* | *540n* | *6µ* | *1µ* | *255n* | *367n* |
| *Area [mm$^2$]* | *0.078* | *0.04* | *0.009* | *0.005* | *0.012* |

TABLE I- ADC COMPARISON WITH PRIOR ART, *-SIMULATED DATA.

| *Interface* | *[1]* | *[2]* | *[3]* | *[4]* | ***[this work]**** |
|---|---|---|---|---|---|
| *Technology* | *0.18* | *0.13* | *0.18* | *0.065* | *0.065* |
| *$V_{DD}$ [V]* | *0.45* | *1.2* | *1.8* | *1* | *1* |
| *Gain [dB]* | *52* | *54-60* | *30-72* | *52.1* | *65* |
| *INF [µ$V_{rms}$]* | *3.2* | *4.7* | *3.2* | *4.13* | *3.1* |
| *Bandw. [Hz]* | *10k* | *10-5k* | *300-6k* | *1-8.2k* | *20k* |
| *P/chann.[µW]* | *0.73* | *3.5* | *5.4* | *2.8* | *2.1* |
| *A/chann.[mm$^2$]* | *0.2* | *0.09* | *0.08* | *0.042* | *0.036* |

TABLE II- NEURAL INTERFACE COMPARISON WITH PRIOR ART, *-SIMULATED DATA.

## IV. CONCLUSION

The increasing density and the miniaturization of the functional blocks in the multi-electrode arrays presents significant circuit design challenge in terms of area, bandwidth, power, and the programmability and expandability of the recording system. In this paper, a low-power, neural recording interface with current-mode SAR ADC is presented. The power consumption is scaled with the input current level making the current mode A/D converter suitable for low energy signals. With the figure of merit of the 14 fJ/conversion-step, and THD of 63.4 dB at 40 kS/s sampling frequency, implemented A/D converter is one of the best reported. The total system consumes only 2.1 µW/channel, and occupy an area of 0.036 mm$^2$/per channel in a 65 nm CMOS technology.

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