

Sensitivity Computation Using Domain-Decomposition for Boundary Element Method Based Capacitance Extractors

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Abstract— The on-going reduction of the on-chip feature size goes together with an increase of process variability. While the manufacturer is expected to improve the uniformity of its output, and the designers are expected to enhance circuit adaptability and reliability, the design tools are expected to deliver convenient and fast approaches capable of giving accurate characterizations of manufacturing tolerances. In this paper, we present an algorithm that enables an extension of 3-D capacitance extractors to generate both the nominal capacitances and their sensitivities w.r.t. all geometric parameters with only one extraction. Using the domain-decomposition technique, it is shown that sensitivities can be derived from the intermediate data of the standard capacitance extraction using the Boundary Element Method (BEM). The algorithm has been implemented in a layout-to-circuit extractor. It is shown by experiments that the additional cost for the sensitivity computation is less than 20% of the standard time consumption, essentially independent of the number of parameters.

I. INTRODUCTION

Accurate capacitance extraction is essential for signal integrity analysis of IC interconnects. However, as already broadly acknowledged, the technology-scaling and the increase in process complexity are introducing significant variabilities such that the relative impact of interconnect delay is greatly enlarged.

One possible approach to deal with these variabilities is to use sensitivities of the electrical elements with respect to process parameters. These sensitivities are necessary for establishing basic formulations in various variation-aware algorithms, such as moment-based timing analysis [1], Hermite polynomial based statistic analysis [2] and parametric Model Order Reduction (pMOR) proposed in [3]. Also, techniques including fast corner generation, multi corner extraction and the variation-aware Static Timing Analysis (STA) presented in [4] are all based on sensitivity models. The Standard Parasitic Exchange Format (SPEF) has been extended to incorporate sensitivities for process and temperature variations. The new sensitivity-based SPEF format enables extraction tools to generate a netlist with nominal values of parasitics and their sensitivities, which can be easily read by subsequent tools for analysis.

In this paper, we will present a sensitivity computation algorithm for BEM based capacitance extractors. The algorithm is very efficient in the sense that the nominal capacitances and their sensitivities can be generated with *one single* 3-D extraction. The rest of the paper is organized as follows. Section II starts by giving some preliminary information about the so-called *partial short-circuit capacitances*. Then we show that simply with these capacitances, sensitivities can be computed using the domain-decomposition technique. Section III gives complexity analysis of the algorithm based on the implementation in a circuit-to-layout extractor. Two realistic experiments are presented in Section IV. Numerical results demonstrate the accuracy and the efficiency of our algorithm with concrete numbers. This

is followed by a statistical application of sensitivities. At last, Section V concludes the paper.

II. ALGORITHM DERIVATION

A. Background

Capacitances used in SPICE netlists are in fact called *network capacitances* (\mathbf{C}) and can be specified in terms of the so-called *short-circuit capacitances* (\mathbf{C}_s) based on the following relevance:

$$C_{ij} = -C_{sij} \quad \forall i \neq j \quad (1a)$$

$$C_{ii} = \sum_{j=1}^N C_{sij} \quad \forall i = 1, 2, \dots, N \quad (1b)$$

where C_{ij} is the coupling capacitance between conductors i and j ; C_{ii} is the ground capacitance of conductor i . The entry of the short-circuit capacitance matrix C_{sij} is equal to the charge on conductor i when conductor j is held at a unit potential and all other conductors are short-circuited to the ground.

When the BEM is used for capacitance extraction, conductor surfaces are discretized into panels. The short-circuit capacitances associated to the discretized panels before their association to conductors are called *partial short-circuit capacitances*, denoted $\bar{\mathbf{C}}_s$ in this paper. The matrix $\bar{\mathbf{C}}_s$ is given by the inversion of the *Green's function matrix* \mathbf{G} , whose entry G_{ij} amounts to the potential induced at panel i by the charge at panel j .

B. Domain-Decomposition

We will now discuss how the domain-decomposition technique can be applied to determine capacitance sensitivities. Consider Figure 1(a), which shows a cross-section of a metal conductor N_1 , with capacitive couplings to other conductors. Assume that we are interested in the sensitivities of all the capacitances w.r.t. the movement of the rightmost panel of the conductor. As shown in Figure 1(b), the rightmost panel is moved inward by $-d$ (by convention, d is taken negative for an inward displacement). By moving the panel, all capacitances in the figure will change.

To find out how much the capacitances will change, we apply domain-decomposition to Figure 1(b), obtaining Figure 1(c). As shown, a virtual panel is placed at the original location of the panel, making all the outer capacitances equal to the capacitances in the original model. The only difference is the capacitance that now appears inside conductor N_1 .

Since we are computing sensitivities, d is actually infinitesimally small. Therefore there will only be a significant capacitance between the translated panel and the virtual panel. This capacitance can be computed simply from the parallel-plate formula $\Delta C = -\varepsilon A/d$, where ε is the material permittivity

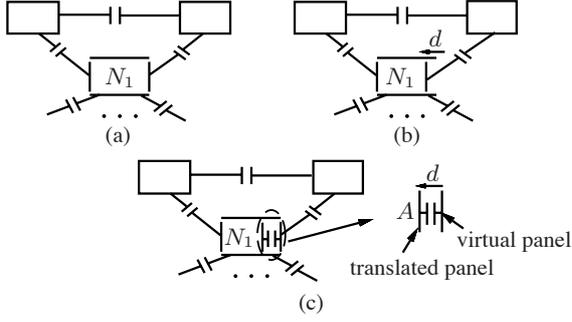


Fig. 1. Applying domain-decomposition to find capacitance sensitivities. around the panel, A is the area of the panel and the minus sign comes from the fact that the panel is moved inward.

Now, to see how the other capacitances will change, we write down the partial short-circuit capacitance matrix,

$$\bar{\mathbf{C}}'_s = \begin{bmatrix} \bar{C}_{s11} & 0 & \bar{\mathbf{C}}_{s1x} \\ 0 & 0 & \mathbf{0} \\ \bar{\mathbf{C}}_{s1x}^T & \mathbf{0} & \bar{\mathbf{C}}_{sxx} \end{bmatrix} + \begin{bmatrix} \Delta C & -\Delta C & \mathbf{0} \\ -\Delta C & \Delta C & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \quad (2)$$

which is a block-matrix, partitioned as

$$\begin{bmatrix} 1 \times 1 & 1 \times 1 & 1 \times m \\ 1 \times 1 & 1 \times 1 & 1 \times m \\ m \times 1 & m \times 1 & m \times m \end{bmatrix} \quad (3)$$

where m is the number of surrounding panels. The first node (first row and column) in this matrix corresponds to the virtual panel in Figure 1(c), and the second node corresponds to the translated panel. The row-vector $\bar{\mathbf{C}}_{s1x}$ represents the couplings from the virtual panel to the surrounding panels, and the matrix $\bar{\mathbf{C}}_{sxx}$ represents the couplings among the surrounding panels and their ground capacitances. Note that the second term in (2) is the ‘‘MNA-stamp’’ which implements the parallel plate capacitor between the translated and the virtual panel. For clarity, we point out that the original partial short-circuit capacitance matrix before the panel displacement is

$$\bar{\mathbf{C}}_s^0 = \begin{bmatrix} \bar{C}_{s11} & \bar{\mathbf{C}}_{s1x} \\ \bar{\mathbf{C}}_{s1x}^T & \bar{\mathbf{C}}_{sxx} \end{bmatrix} \quad (4)$$

where the entries are the same as the ones in the first term in (2).

We proceed by eliminating the first node in $\bar{\mathbf{C}}'_s$ by taking its Schur complement, giving

$$\bar{\mathbf{C}}_s = \begin{bmatrix} \Delta C & \mathbf{0} \\ \mathbf{0} & \bar{\mathbf{C}}_{sxx} \end{bmatrix} - \frac{1}{\bar{C}_{s11} + \Delta C} \begin{bmatrix} -\Delta C \\ \bar{\mathbf{C}}_{s1x}^T \end{bmatrix} \cdot [-\Delta C \quad \bar{\mathbf{C}}_{s1x}] \quad (5)$$

or, collecting terms,

$$\bar{\mathbf{C}}_s = \begin{bmatrix} \frac{\bar{C}_{s11}\Delta C}{\bar{C}_{s11} + \Delta C} & \frac{\bar{\mathbf{C}}_{s1x}\Delta C}{\bar{C}_{s11} + \Delta C} \\ \frac{\bar{\mathbf{C}}_{s1x}^T\Delta C}{\bar{C}_{s11} + \Delta C} & \bar{\mathbf{C}}_{sxx} - \frac{\bar{\mathbf{C}}_{s1x}^T\bar{\mathbf{C}}_{s1x}}{\bar{C}_{s11} + \Delta C} \end{bmatrix}. \quad (6)$$

Substituting the parallel-plate formula $\Delta C = -\varepsilon A/d$ into (6) and taking the derivative w.r.t. d gives us

$$\frac{\partial \bar{\mathbf{C}}_s}{\partial d} = \frac{\varepsilon A}{(\varepsilon A - \bar{C}_{s11}d)^2} \begin{bmatrix} \bar{C}_{s11}^2 & \bar{C}_{s11}\bar{\mathbf{C}}_{s1x} \\ \bar{C}_{s11}\bar{\mathbf{C}}_{s1x}^T & \bar{\mathbf{C}}_{s1x}^T\bar{\mathbf{C}}_{s1x} \end{bmatrix}. \quad (7)$$

Since we are interested in the sensitivity at $d = 0$, we may simplify this as

$$\frac{\partial \bar{\mathbf{C}}_s}{\partial d} = \frac{1}{\varepsilon A} \begin{bmatrix} \bar{C}_{s11}^2 & \bar{C}_{s11}\bar{\mathbf{C}}_{s1x} \\ \bar{C}_{s11}\bar{\mathbf{C}}_{s1x}^T & \bar{\mathbf{C}}_{s1x}^T\bar{\mathbf{C}}_{s1x} \end{bmatrix}. \quad (8)$$

An entry of the above sensitivity matrix (8) can subsequently be written as

$$\frac{\partial \bar{C}_{sab}}{\partial d} = \frac{\bar{C}_{s1a}\bar{C}_{s1b}}{\varepsilon A} \quad (9)$$

where a and b can be any panels including the translated one. This expression shows that the sensitivity between two panels w.r.t. d can be computed by their couplings to the virtual panel. And these couplings can directly be obtained from the original partial short-circuit capacitance matrix $\bar{\mathbf{C}}_s^0$. Note that for BEM based extractors, capacitances are also computed from the matrix $\bar{\mathbf{C}}_s^0$. Therefore the sensitivities can be computed along with the extraction of capacitances on-the-fly. This is a key result of our algorithm. It explains why we can obtain both capacitances and their sensitivities with only one system solve.

In the following, we will show how (9) is used to obtain the final capacitance sensitivities between conductors. First, we sum over all panels that belong to the same conductor. The sensitivity of coupling (short-circuit) capacitance between conductors i and j can therefore be written as

$$\frac{\partial C_{sij}}{\partial d} = \frac{1}{\varepsilon A} \sum_{a \in N_i} \sum_{b \in N_j} \bar{C}_{s1a}\bar{C}_{s1b}. \quad (10)$$

Then we consider a geometric parameter p with a nominal value p_0 , and d is actually $(p - p_0)$. Hence,

$$\frac{\partial C_{sij}}{\partial d} \Big|_{d=0} = \frac{\partial C_{sij}}{\partial (p - p_0)} \Big|_{p=p_0} = \frac{\partial C_{sij}}{\partial p} \Big|_{p=p_0}. \quad (11)$$

Until now we worked with the short-circuit capacitances and they need to be converted into network capacitances using (1a). Thus the coupling capacitance sensitivity w.r.t. parameter p , using (11), becomes

$$\frac{\partial C_{ij}}{\partial p} = -\frac{1}{\varepsilon A} \sum_{a \in N_i} \sum_{b \in N_j} \bar{C}_{s1a}\bar{C}_{s1b}. \quad (12)$$

For simplicity reasons, we only considered one moving panel in the above discussion while actually there is a set of panels on the moving surface incident to d (or parameter p). We will call them the *victim panels* in the rest of this paper. The Schur complement of a matrix block is then used to deal with the multiple victim panels. Details of the derivation, due to the lack of space here, can be found in [5]. Basically we can accumulate the victim panels and reach the final equation for the capacitance sensitivity between conductors i and j :

$$\frac{\partial C_{ij}}{\partial p} = -\sum_{k \in s_p} \left(\frac{1}{\varepsilon A_k} \sum_{a \in N_i} \sum_{b \in N_j} \bar{C}_{s_k,a}\bar{C}_{s_k,b} \right) \quad (13)$$

where s_p is the set of victim panels incident to p . This description shows that sensitivities w.r.t. different parameters are simply incident to different sets of victim panels. All the sensitivities w.r.t. multiple parameters can be computed simultaneously once the associated partial short-circuit capacitances are available.

Analogically, the sensitivity for the ground capacitance can be derived and written as follows

$$\frac{\partial C_{ii}}{\partial p} = \sum_{k \in s_p} \frac{1}{\varepsilon A_k} \sum_{a \in N_i} \bar{C}_{s_k, a} \left(\sum_{j=1}^N \sum_{b \in N_j} \bar{C}_{s_k, b} \right). \quad (14)$$

III. COMPLEXITY ANALYSIS

The algorithm is implemented in, while not limited to, a layout-to-circuit extractor SPACE [6] using C++. Complexity analysis based on this implementation is given in this section. Due to the lack of space here, we will present the main results, while more detailed explanation can be found in [7] and [5].

The time consumption for capacitance extraction without using any acceleration technique, is $O(m^3)$, with m the total number of panels. The additional computational burden for sensitivity computation using our algorithm is $O(m^2) + O(nN^2)$, where n is the number of victim panels and N is the number of conductors. Since $n \leq m$ and normally $N \ll m$, $O(m^2)$ is the major cost for the sensitivity computation. Compared to the complexity of standard capacitance extraction $O(m^3)$, the additional cost $O(m^2 + nN^2)$ is negligible. For the memory complexity, the standard capacitance extraction is $O(m^2)$. The extra storage cost for sensitivities is $O(MN^2 + m)$ with M the number of parameters ($M \ll m$), which is also negligible compared to the complexity of $O(m^2)$.

However the complexities of both the time consumption and the memory cost are too high to be used in practice. This problem can be solved by using the *windowing* technique in SPACE. This technique is based on the fact that when two panels are far enough away from each other, their capacitive coupling can be small enough to be neglected. The window size w is the threshold for distinguishing whether this coupling should be considered or not. If the distance between the pair is larger than $2w$, their capacitance will not be counted. Using the windowing technique, the time complexity for the standard capacitance extraction is reduced to $O(mw^4)$. In this case, the major cost for the sensitivity computation is equal to $O(p_w^2 n_w)$, with p_w being the number of panels within one window and n_w the number of windows in the layout. Since in realistic layout, $p_w = O(w^2)$ and $n_w = O(m/w^2)$, the major time consumption for sensitivities amounts to $O(mw^2)$. Also, the memory cost of standard capacitance extraction is reduced to $O(w^4)$. The cost for the sensitivities becomes $O(MN_w^2 + w^2)$, where N_w ($N_w \ll w$) is the number of conductors within one window. Therefore, the extra time and memory costs for computing sensitivities are essentially negligible compared to the complexities for the standard capacitance extraction.

IV. EXPERIMENTS AND RESULTS

A. Accuracy Verification

Experiments have been conducted on a 2.66GHz Intel Xeon CPU with 1GB memory. The first experiment is a 2-by-2 interconnect structure of which the dimensions are shown in Figure 2. Since the structure is symmetrical, three coupling capacitances (C_{f12} , C_{s12} , C_{fs}) and two ground capacitances (C_{fgnd} , C_{sgnd}) are studied. For each layer, we consider three parameters, namely the layout variation (l_i , $i = 0, 1$), the thickness of the metal (t_i , $i = 0, 1$) and the height of the

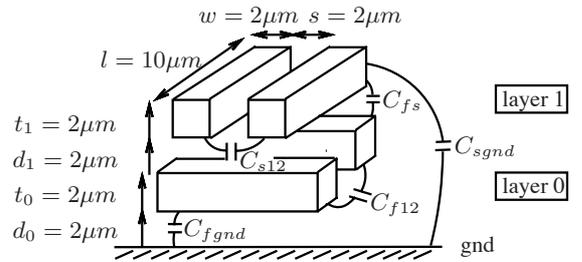


Fig. 2. 3-D representation of a 2-by-2 interconnect structure.

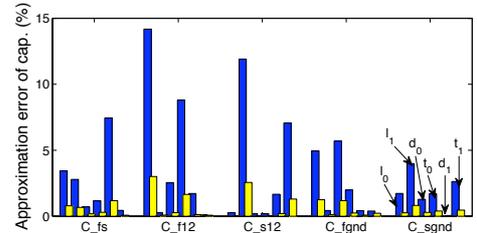


Fig. 3. Comparison between 0^{th} order and 1^{st} order approximations. Each group of two bars, one in blue (0^{th} order approx.) and one in yellow (1^{st} order approx.), represents the errors of capacitances for one parameter. The six parameters are, in sequence, l_0 , l_1 , d_0 , t_0 , d_1 , t_1 .

dielectric (d_i , $i = 0, 1$). Assuming a 10% variation in each parameter, we model the capacitances with 1^{st} order (i.e. linear) approximations using the sensitivities given by our algorithm. Then we manually change the dimensions of the structure accordingly by 10% and the extracted capacitances will serve as a reference.

Figure 3 shows the comparison between the 0^{th} order and the 1^{st} order approximations where the 0^{th} order is equivalent to the situation in which variability is not accounted for. Several observations can be made:

- 1) Process variations can not be simply neglected; some can introduce errors of capacitances exceeding 10%.
- 2) The 1^{st} order approximation improves much over the 0^{th} order approximation. For instance, under a 10% variation in l_0 , the 0^{th} order of coupling capacitance C_{f12} gives an error of almost 15%, which drops to 3% using the 1^{st} order approximation.
- 3) The computed sensitivities have an acceptable accuracy indicated by the small errors of the 1^{st} order approximations (the maximum error is less than 3%).
- 4) For each capacitance, not all parameter variations are influential; some of them are even barely noticeable.

To further show the accuracy of the sensitivity computation, we construct a 2^{nd} order polynomial fit of the extracted capacitances, i.e., $C(p) = a_0 + a_1 p + a_2 p^2$ for every parameter. Then we take its derivative at the nominal dimension p_0 , i.e., $2a_2 p_0 + a_1$ as the reference for sensitivities. Here we study the sensitivities incident to capacitances with 0^{th} order errors larger than 5%. The average error of these sensitivities compared to the references is 15.16%. This error can come from the fact that only the translated panels are considered in our algorithm (see Figure 1), while the change of the panel size (e.g., the top and the bottom panels of N_1) is not accounted for. Further study on this is still undertaken. However, since the sensitivity itself is a second-order effect to the capacitance, an accuracy

TABLE I

COMPARISON OF THE STANDARD DEVIATIONS GIVEN BY THE ESTIMATION FROM MONTE-CARLO SAMPLE DATA (LEFT COLUMN) AND THE COMPUTATION RESULT OF THE LINEAR MODEL (MIDDLE COLUMN).

	normfit (F)	model (F)	error
σ_{fs}	$8.94e-18$	$8.19e-18$	8.40%
σ_{f12}	$25.81e-18$	$23.38e-18$	9.41%
σ_{s12}	$27.75e-18$	$25.70e-18$	7.39%
σ_{fgnd}	$29.64e-18$	$26.03e-18$	12.19%
σ_{sgnd}	$11.60e-18$	$9.89e-18$	14.70%

of better than 20% should be good enough for the sensitivity computation.

B. Statistical Application of Sensitivities

In this section, we will illustrate one possible application of sensitivities in statistical analysis. Based on the sensitivities given by our algorithm, we can immediately obtain the standard deviations of capacitances given the statistical assumption of the geometric parameters. The accuracy is verified by a Monte-Carlo simulation of an experimental layout. Finally, comparisons of the time consumption are given.

We start by establishing a linear model of capacitance C :

$$C = C_0 + \sum_i \frac{\partial C}{\partial p_i} \Delta p_i. \quad (15)$$

Normally, the technology part can provide statistical distributions of the parameters. Therefore once the sensitivities are computed, we can derive the statistical distribution of C . For instance, we assume that there are n Gaussian distributed parameters. Due to the linearity of (15), C is also Gaussian with a mean C_0 and a variance given as following

$$\sigma_C^2 = \sum_{i=1}^n \left(\frac{\partial C}{\partial p_i} \sigma_{p_i} \right)^2. \quad (16)$$

Hence the standard deviation of a capacitance (σ_C) can easily be computed using the sensitivities given by our algorithm.

To check the accuracy of these computed sigmas, we perform 1000 Monte Carlo samplings on the same 2-by-2 interconnect structure as in the previous section. Parameter p_i ($i = 1, \dots, 6$) is assumed to be Gaussian with a mean (μ_{p_i}) of its nominal value and the 3-sigma tolerance ($3\sigma_{p_i}$) being 10% of μ_{p_i} .

The output capacitance samplings are proven to be Gaussian distributed with a Lilliefors test using the Matlab command *lillietest* at a 5% confidence level. This also agrees with the linearity assumption. Then we use another Matlab command *normfit* to estimate, at 95% confidence intervals, the standard deviation of the sample data. The result, used as a reference, is shown in Table I, in comparison to the sigmas given by (16). As shown in the table, the computed sigmas have good enough accuracies, which also implies the accuracy of the computed sensitivities. More importantly, it takes only 23 seconds to get the nominal capacitances and their standard deviations based on the sensitivities and the linear model, while the Monte-Carlo simulation consumes 21 hours and 43 minutes.

The other experiment is conducted on a 3-metal layer interconnect structure. There are 120 capacitances, 105 being the coupling capacitances and 15 the ground capacitances. In this case, there are 9 parameters and in total 1080 capacitance sensitivities. Again we assume the parameters are Gaussian with a 3-sigma being 10% of the mean.

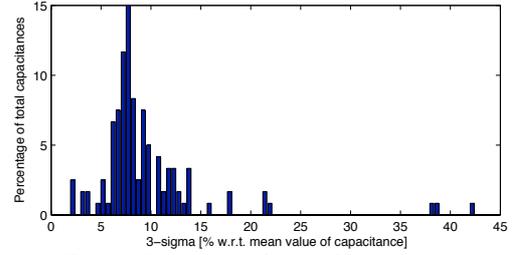


Fig. 4. Percentage of total 120 capacitances.

We compute the 3σ for every capacitance according to (16). To study the effect of geometric variations on capacitances from a statistical point of view, we partition the range of the 3σ which is expressed in percentage of the mean value of each capacitance; and plot the percentage of capacitances in each bin (Figure 4). While most of the 3σ values are less than 15%, we do notice that there are a few of them being around 40%. However, after looking into the numbers we found out that the nominal values of these capacitances are small enough, compared to other capacitances, to be neglected.

The total CPU time for this extraction including the sensitivities is 228.6s. Compared to the time for a standard 3-D extraction on the same configuration being 200.9s, the additional cost for the sensitivity computation is only 27.7s, counting for 13.94% of the standard time consumption. In comparison, Cadence uses another technique to construct capacitance sensitivity models for the fast corner generation and 10% extra time is needed to generate sensitivity models per parameter per layer [4]. Hence for their method, it would take in total 90% additional time to generate all the sensitivity models for this structure. The method presented in this paper is much more efficient.

V. CONCLUSION

This paper addressed an algorithm to compute capacitance sensitivities w.r.t. multiple geometric parameters using domain-decomposition. We have proved, analytically and numerically, that the algorithm is highly efficient in the sense that all the sensitivities can be generated along with the nominal values under one 3-D capacitance extraction with a very modest computation time. Its accuracy has been shown by realistic testing results. The conducted experiments demonstrate that the method can be easily used in conjunction with statistical analysis.

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