LT Codes for Reliable Network-on-Chip Communications

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Abstract—**The concept of Network-on-Chip (NoC) is becoming a main trend in the area of System-on-Chip (SoC) design. In NoC communications, data may have errors caused by noise or technology. Forward-Error-Correction (FEC) algorithms can be used to improve the systems' reliability by detecting and correcting errors on the receivers. Many FEC algorithms were proposed and investigated during the past few decades, but the realization of these FEC algorithms in hardware is still an exciting research area. Hardware-based implementations can be several orders of magnitudes faster than software-based methods so it is interesting to see what kind of FEC scheme can be implemented on hardware environment and how well it works.**

Index Terms—**Hardware, LT Codes, Network-on-Chip.**

I. INTRODUCTION

In this paper, the LT Codes[1] that originate from the new coding family of the Digital Fountain Codes have been studied. In this algorithm, a sparse random parity-check graph is dynamically generated at both encoder and decoder to recover the transmitted messages. The LT Codes are also known as the first realization of rateless codes, which can generate potentially limitless codeword symbols from original data and can self-adjust to channels with different behaviors. LT Codes also have a very low encoding/decoding cost when compared with some traditional block codes, e.g. Reed Solomon (RS) codes and Low-Density-Parity-Check (LDPC) codes. Therefore, LT Codes are very suitable for multi-channel environments such as NoC network architecture.

Two Binary Erasure Channel (BEC)[2] models are proposed in different OSI layers and are used to analyze the performance of LT Codes. An efficient hardware implementation of the LT coder is presented, based on the LDPC coder described in [3]. The hardware architecture is improved to achieve nearly linear encoding and decoding time complexity.

II. NETWORK ON CHIP (NOC)

With the introduction of Nano-technology, integration density of a System-on-Chip (SoC) is not limited by the individual IP block size but by the on-chip communication structures. For these complex systems, the concept of Network-on-Chip (NoC) was introduced to provide flexible and scalable communication architecture. However in the Nano world, NoC communication is not error free due to various reasons such as noise interference and technology effects.
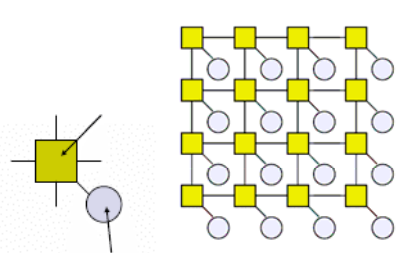

Figure 1. A NoC system based on the 2-D mesh network architecture.

III. LT CODES

Forward-Error-Correcting (FEC) can be used to improve the NoC reliability by introducing additional bits and correct the errors at receivers. LT Codes is the first realization of the new FEC family, the Digital Fountain Codes, which is also known as the rate-less codes. When compared with the traditional block codes, LT codes have several advantages:

- LT codes are based on bitwise operations
- LT codes can adapt to different channel behavior and minimize overhead
- The performance is very close to the Shannon Limit

	LT Codes	RS Codes
Complexity	$O(n*log(n))$	$O(n^2)$
Overhead	Non-fixed	Fixed
Basic Operations	XOR	Field Operation

Figure 2. LT Codes versus Reed-Solomon (RS) Codes.

Figure 3 shows the LT codes' code rate for different channel error rates. Instead of a vertical line for fixed-rate codes such as RS codes, the code rate changes with the channel behavior.
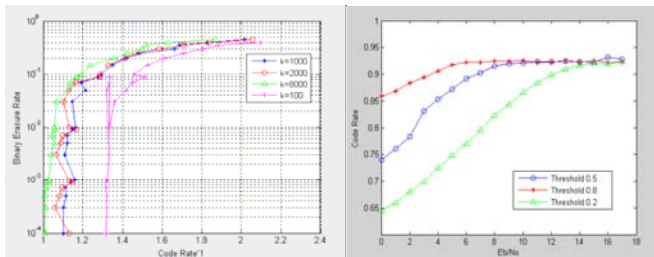

Figure 3. LT Code rate vs. Binary Erasure Rate on BEC and LT Code rate vs. SNR on AWGN.

IV. HARDWARE ARCHITECTURE OF THE LT CODER

LT Codes are based on low-density matrix computing. The main steps of the LT coding algorithm are:
- LT degree distribution generation
- Low density matrix generation at both sender and receiver
- LT encoding (matrix-vector multiplication)
- LT decoding (Belief propagation process)

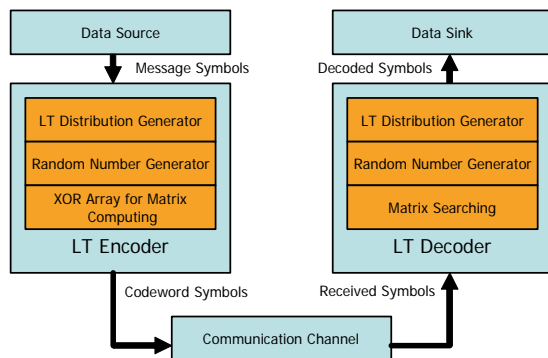Figure 4 shows the block diagram of an LT coding system.

Figure 4. Block Diagram of LT Coder.

The LT Coding scheme can be implemented with simple hardware components. Figure 5 shows the LT encoding algorithm implemented by an XOR gate array.
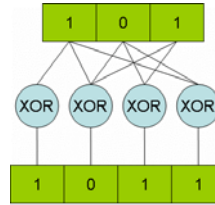

Figure 5. LT Encoding Scheme.

V. COMMUNICATION CHANNEL MODELS

Initially, LT codes are designed to be used for Binary Erasure Channels (BEC). A channel model can be derived by modifying the modulation method on the data- link layer. Figure 6 shows the Binary Error Rate versus Signal-Noise-Ratio curve of a BEC model based on an Additive—White-Gaussian-Noise (AWGN) channel and on modified Binary-Phase-Shift-Key (BPSK) modulation.
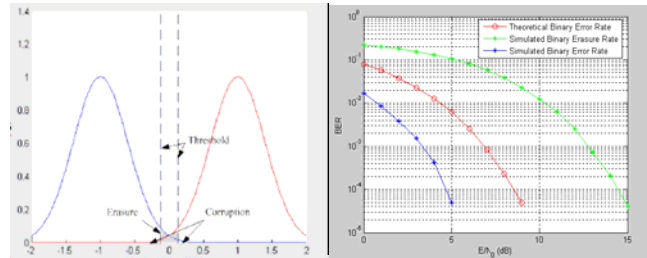

Figure 6. Modified BPSK Modulation and the BER versus SNR curve on the Binary Erasure Channel Model.

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