Analysis of timing resolution of a digital silicon photomultiplier.

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I. Abstract

This paper presents the analysis of timing resolution for a digital silicon photomultiplier (D-SiPM) using a SPICE simulator. A D-SiPM has more than a hundred of pico seconds timing resolution for single-photon detection due to detector jitter, circuit noise and routing skew. Especially, circuit noise and skew depend on the SiPM design strongly. To investigate how single-photon timing resolution is related to architectural choices and design parameters, we have simulated the timing resolution by sweeping the design parameters: the transistor size and the transistor channel length, wire resistance and capacitance. We considered D-SiPMs of different sizes and with a variety of signal distribution architectures.

II. Introduction

Silicon photomultipliers (SiPMs) are an alternative to photomultiplier tubes (PMTs) because of their robustness to magnetic fields, compactness, and low bias voltage [1]. An analog SiPM (A-SiPM) consists of an array of avalanche photodiodes operating in Geiger mode (single-photon avalanche diodes, SPADs), whose avalanche currents are summed in one node, and the output will be processed with off-chip components as shown in Fig. 1 (a) [1]. In digital SiPMs (D-SiPMs) on the contrary, all of the SPAD outputs are combined together by means of a digital OR, and the output is directly routed to an on-chip time-to-digital converter (TDC) to reduce external components and temporal noise as shown in Fig. 1 (b) [2], [3]. Timing resolution for single-photon detection is limited by SPAD jitter and circuit noise, as well as systematic skew due to imperfectly balanced routing. This paper investigates how single-photon timing resolution is related to architectural choices and design parameters. Design parameters include the transistor size and the transistor channel length, wire resistance and capacitance, assuming that the D-SiPM is implemented in 0.35 μm standard CMOS process with spatial random process variations for the transistor channel length and wire resistance and capacitance [4]. We considered D-SiPMs of different sizes and with a variety of signal distribution architectures.

III. Skew

When photons hit a SiPM, the first photon can arrive at any SPAD spatially at random. Thus the timing resolution degrades due to routing skew. H-tree is a well known topology for a clock signal to minimize the skew, and it is applicable to a D-SiPM with an OR gate in each junction. As shown in Fig. 2 (a), H-tree is implemented from each SPAD to the timing output via a buffer and 2-input OR gates. We assume that the SPAD pitch and unit wire length is 50 μm and 25 μm, respectively, the number of SPADs is 64 × 64. In H-tree design, determination of the maximum transition time is important for skew control, area and power dissipation [5]. We use a parameter $\lambda = C_{out}/C_{in}$ to control the transition time, where C_{in} is the input capacitance of the OR gate and C_{out} is its output load capacitance to drive the next stage including the input capacitance of the next OR gate [6]. λ at Nth junction is defined using the unit wire capacitance, C_w, as,

$$\lambda = C_{out}/C_{in} = (C_w \times 2^{N/2} + C_{in(N+1)})/C_{in(N)}. \quad (1)$$

The output of the H-tree is connected to a unit size OR gate to minimize the input capacitance, so $C_{in(13)}$ is a known value. Therefore, all C_{in} will be calculated successively. Fig. 3 and Fig. 4 show the propagation delay and skew for each λ varying C_w from 7 fF to 2 fF, and the unit wire resistance, R_w, from 3.5 ohm to 1 ohm, respectively, assuming that each transistor channel length (L_{tr}), unit wire capacitance, and unit wire resistance has 5 % sigma process variation. Both the propagation delay and the skew improve dramatically by changing λ from 7 to 2 while the transistor area occupies 4.5 times larger. One future option could be designing the D-SiPM using an advanced CMOS process, such as 180 nm, 130 nm or 90 nm, not to have big impact on the D-SiPM fill factor. Note that that C_w has more effect on the skew than R_w in the case of D-SiPMs, while R_w is very important for A-SiPMs [7]. The process variation for L_{tr}, C_w and R_w were set to vary from 5 % to 1% to see the dominant factor for the skew as shown in Fig. 5, thus demonstrating that L_{tr} has the highest impact on the skew.

IV. Temporal noise

The temporal noise of the D-SiPM is composed of SPAD jitter, σ_{spad}, and the noise by the timing signal routing, σ_{route}, including transistor induced noise and kTC noise [8]. The temporal noise model is shown in Fig. 6 (a). Assuming that all these sources of noise are wide-sense stationary, statistically independent random processes with gaussian distribution, the total standard deviation of the resulting process is computed as,

$$\sigma^2_{jitter} = \sigma^2_{spad} + \sigma^2_{route}. \quad (2)$$

Fig. 6 (b) shows simulation results of the noise by routing, σ_{route}, and the total temporal noise, $\sigma_{spad+route}$, assuming

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that the SPAD jitter is 42.6 ps sigma [3]. It is observed that the SPAD jitter is dominant for the temporal jitter.

V. Timing resolution of D-SiPMs

Under the same assumption of before, the timing uncertainty of D-SiPMs is calculated as,

$$\sigma_{sipm}^2 = \tau_{skew}^2 + \sigma_{jitter}^2. \quad (3)$$

Fig. 7 (a) shows the timing resolution of the D-SiPM for a range of λ derived from τ_{skew} and σ_{jitter} at 5 % process variation. The timing resolution improves by utilizing small λ because the skew improves. Fig. 7 (b) shows that the timing resolution improves by reducing the transistor channel length variation and approaches to the SPAD jitter. We have also investigated the timing resolution dependency on the size of the D-SiPM. Fig. 8 (a) shows the timing resolution as a function of array size and λ. By reducing the size of the D-SiPM, the D-SiPM will be less sensitive to process variations because the skew becomes small. Therefore, to achieve good timing resolution, the D-SiPM should be divided into small groups of SPADs, and connected to TDCs in another die with short 3-D vias, as shown in Fig. 8 (b), as well as optimizing the value of λ and designing transistors carefully not to have any geometrical asymmetry thus introducing L_{tr} variations.

VI. Conclusion

We have presented the analysis of timing resolution for a D-SiPM using a SPICE simulator. Generally, a D-SiPM has more than a hundred of picoseconds timing resolution for single-photon detection due to detector jitter, circuit noise and routing skew. We found that SPAD jitter and skew have a strong impact on the timing resolution of the D-SiPM, though the timing resolution can be improved by choosing a proper architecture or modifying the design parameters: i.e. transistor width and length, wire resistance and capacitance, and their process variations.

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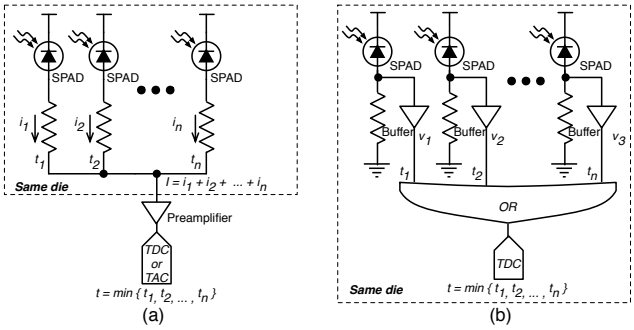

Fig. 1. The concept of (a) an Analog SiPM and (b) a Digital SiPM.

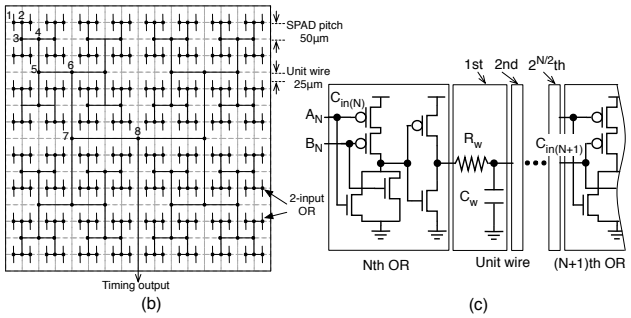

Fig. 2. (a) H-tree for timing signals. (b) Model for the route from Nth junction to (N+1)th junction.

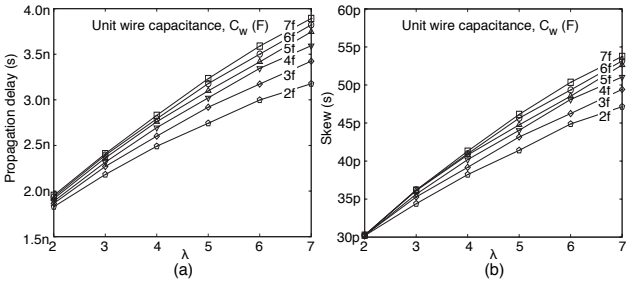

Fig. 3. (a) Propagation delay and (b) skew in various λ values with different values of C_w.

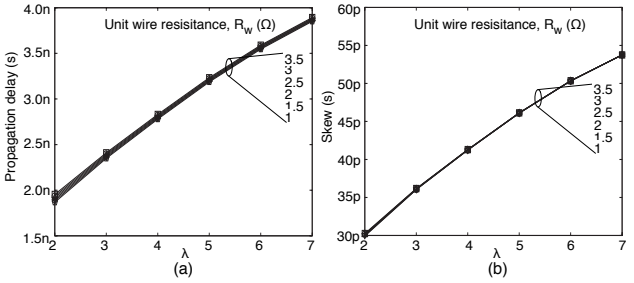

Fig. 4. (a) Propagation delay and (b) skew in various λ with different values of R_w. R_w was found to have negligible effect on propagation delays and skews.

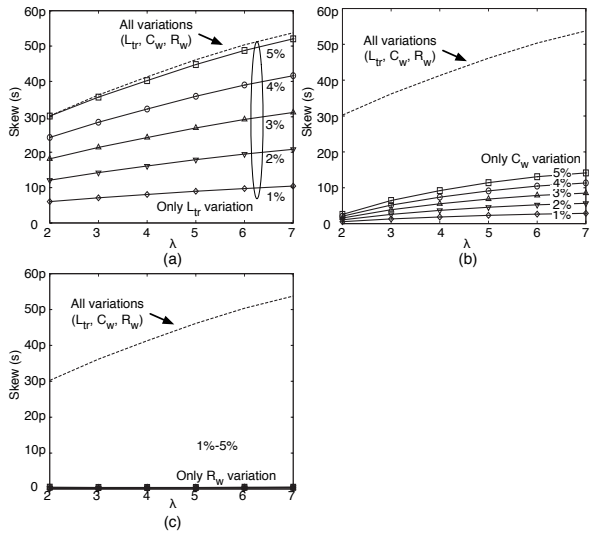

Fig. 5. Skew dependency on (a) L_{tr}, (b) C_w and (c) R_w. For a broken line, the situation that L_{tr}, C_w and R_w has 5% sigma process variation at the same time is considered as a refence.

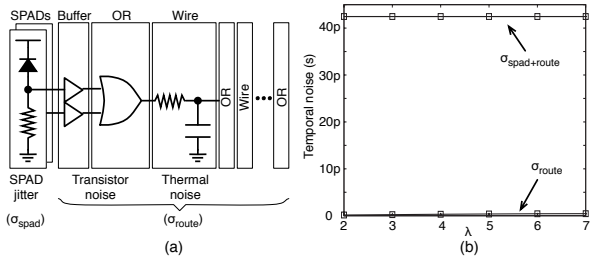

Fig. 6. (a) Temporal noise sources in the D-SiPM. (b) Temporal noise in the D-SiPM in various values of λ.

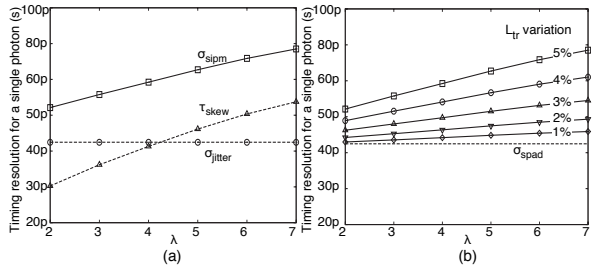

Fig. 7. (a) Timing resolution of a D-SiPM for single-photon detection. (b) Timing resolution with different values of relative L_{tr} variations.

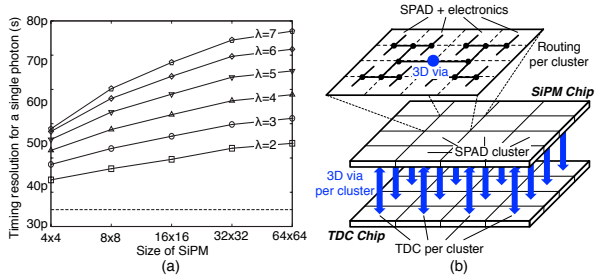

Fig. 8. (a) Timing resolution of the D-SiPM for a single-photon in different sizes of array for the D-SiPM. (b) Ideal configuration of a D-SiPM.