Timing optimization of a H-tree based digital silicon photomultiplier

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Timing optimization of a H-tree based digital silicon photomultiplier

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ABSTRACT: This paper presents a compresensive analysis of timing resolution for a digital silicon photomultiplier (D-SiPM) using a SPICE simulator. Generally, digital silicon photomultipliers (D-SiPMs) have a full-width-half-maximum (FWHM) single-photon timing resolution (SPTR) of more than 100 ps, often of several hundreds picoseconds. This is primarily due to detector jitter, circuit noise, and routing skew. Circuit noise and skew, in turn, strongly depend on the SiPM design; this dependency has been investigated by varying transistor size and transistor channel length, wire resistance, and capacitance. The scalability of the method has been validated by considering D-SiPMs of different sizes and with a variety of signal distribution architectures.

KEYWORDS: Timing detectors; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs etc); Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc); Photon detectors for UV, visible and IR photons (solid-state)

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1 Introduction

Silicon photomultipliers (SiPMs) are a solid-state alternative to photomultiplier tubes (PMTs) because of their robustness to magnetic fields, compactness, and low bias voltage [1]. An analog SiPM (A-SiPM) consists of an array of avalanche photodiodes operating in Geiger mode (single-photon avalanche diodes, SPADs), whose avalanche currents are summed in one node, and the output will be processed with off-chip components as shown in figure 1 (a) [1]. In digital SiPMs (D-SiPMs) on the contrary, all of the SPAD digital outputs are combined together by means of a digital OR, and the output is directly routed to an on-chip time-to-digital converter (TDC) to reduce external components and temporal noise as shown in figure 1 (b) [2–4]. Timing resolution for single-photon detection is limited by SPAD jitter and circuit noise, as well as systematic skew due to imperfectly balanced routing. However, timing resolution of D-SiPMs is not discussed comprehensively yet in literatures even though some papers investigate the timing performance of A-SiPMs [5, 6].

This paper investigates how single-photon timing resolution (SPTR) is related to architectural choices and design parameters. Design parameters include transistor size and transistor channel length, wire resistance and capacitance, assuming that the D-SiPM is implemented in 0.35 μm standard CMOS process with special random process variations for the transistor channel length and wire resistance and capacitance [7]. However, the method can easily be extended to other process without loss of generality. We considered D-SiPMs of different sizes and with a variety of signal distribution architectures, often discussing the effects of architectural choices and other design parameters on timing resolution; both single-photon and multi-photon timing resolution are important to determine the coincident time resolution (CTR) in positron emission tomography (PET).

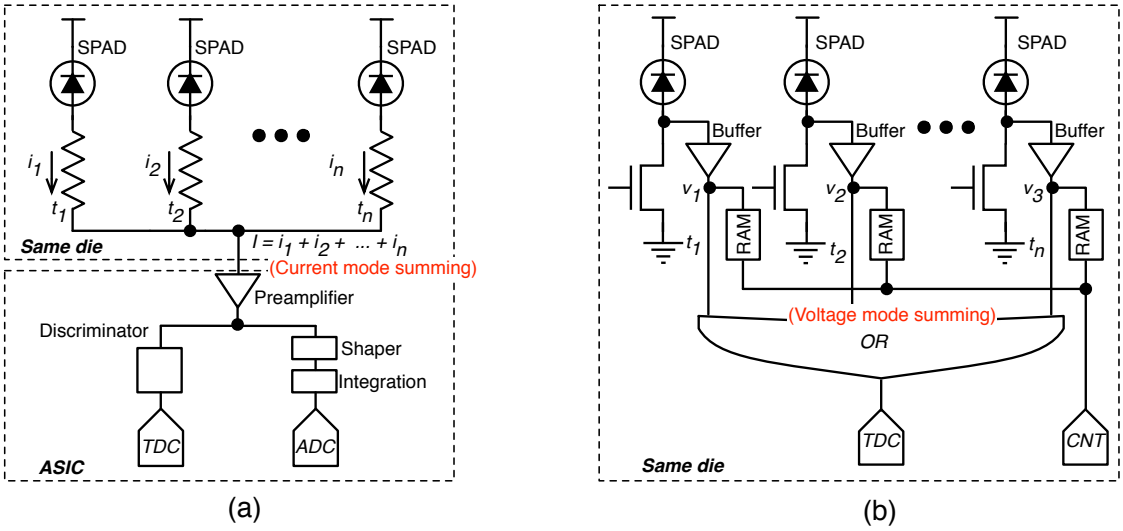

Figure 1. The concept of (a) an Analog SiPM and (b) a Digital SiPM.

The paper is organized as follows. Section 2 shows the structure of the D-SiPM, which was used for our analysis and the definition of swept parameters. In section 3, the simulation results are presented. Finally, conclusions are given in section 4.

2 D-SiPM structure

2.1 D-SiPM configuration

When photons hit a SiPM, the first photon can impinge at any SPAD spatially at random. Thus the timing resolution degrades due to routing skew. H-tree is a well-known topology for a clock signal to minimize skew, and it is applicable to a D-SiPM with an OR gate in each junction. As shown in figure 2 (a), e.g. a 16 $\times$ 16 SPAD array in a D-SiPM, H-tree is implemented from each SPAD to the timing output via a buffer and 2-input OR gates. After a photon hits the n_{th} pixel at time of arrival, T_{ph}, the signal is propagated through a buffer, wires and OR gates, and the time is digitized by a TDC as T_n. The propagation delay and skew, τ_{skew}, is defined as $E(T_n)$ and $\sigma(T_n)$, respectively, as shown in figure 2 (a). Note that the skew is in general the time different between the maximum value and the minimum value, however, we define the skew as a random variable in terms of its standard deviation (sigma). Figure 2 (b) shows the circuit schematic for our simulation. Following a SPAD, a buffer composed by two inverters and unit wires corresponding to the propagation path until the SiPM output inserting an OR gate in each junction. As an unit wire, which is a half length of the pixel pitch, a simple RC model (R_w and C_w) is employed. An OR gate consists of a NAND gate and an inverter. In our simulations, we assume that the SPAD pitch and unit wire length is 50 µm and 25 µm, respectively, the number of SPADs is 64 $\times$ 64.

2.2 D-SiPM design parameters

In H-tree design, determination of the maximum transition time is important for skew control, area and power dissipation [8]. We use a parameter $\lambda = C_{\mathrm{out}}/C_{\mathrm{in}}$ to control the transition time, where

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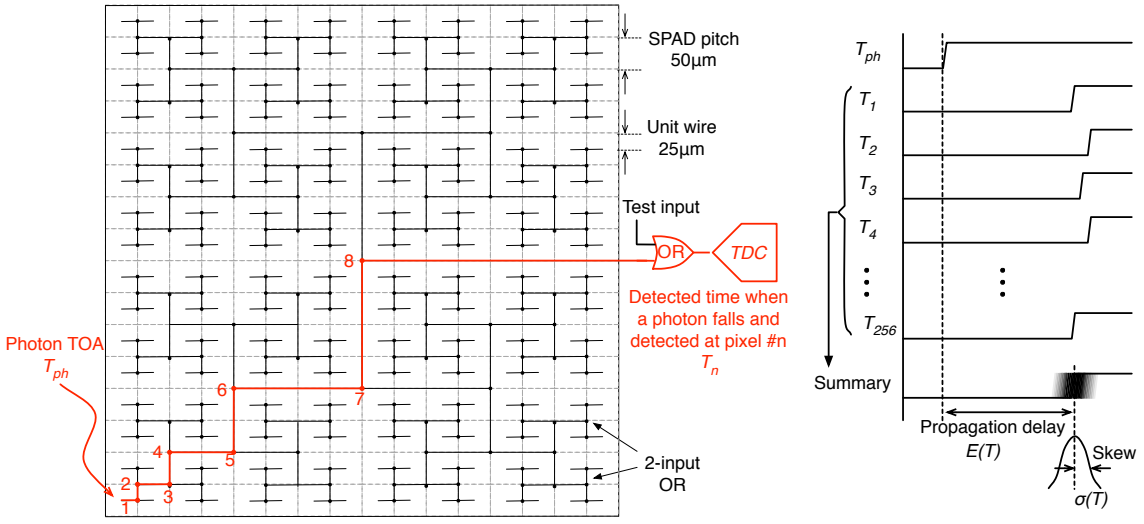
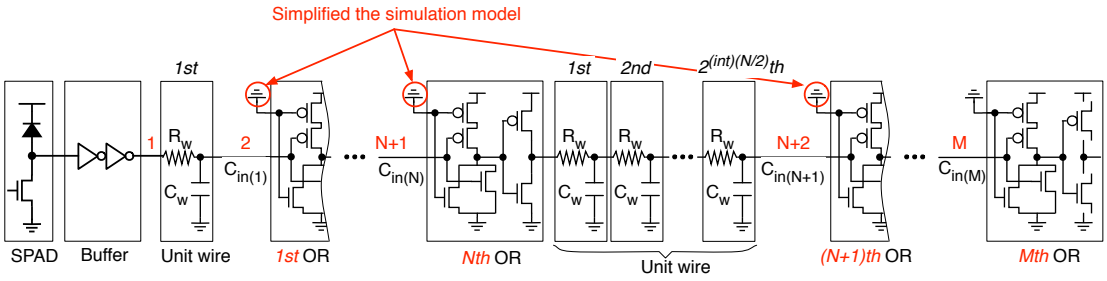


(a)



(b)

		INV1	INV2	OR1	OR2	OR3	OR4	OR5	OR6	OR7	OR8	OR9	OR10	OR11	OR12	OR13
C_{out}/C_{in}	Wire cap(fF)	0	7	7	14	14	28	28	56	56	112	112	224	224	448	0
2	NMOS size (μm)	0.7	1.5	2.0	2.9	3.9	5.8	7.5	11.0	14.0	20.0	24.0	32.1	32.1	32.3	0.5
	PMOS size (μm)	1.2	2.4	6.3	9.4	12.4	18.4	24.0	35.2	44.8	64.1	76.9	102.6	102.8	103.2	1.6
3	NMOS size (μm)	0.2	0.6	0.7	1.1	1.4	2.3	2.9	4.6	5.7	9.0	10.9	16.6	17.8	21.5	0.5
	PMOS size (μm)	0.3	0.9	2.3	3.7	4.6	7.3	9.1	14.6	18.1	28.7	34.8	53.2	57.1	68.8	1.6
4	NMOS size (μm)	0.1	0.4	0.4	0.7	0.9	1.4	1.7	2.9	3.4	5.7	6.8	11.0	12.0	16.1	0.5
	PMOS size (μm)	0.1	0.6	1.4	2.3	2.7	4.6	5.5	9.1	11.0	18.2	21.6	35.2	38.5	51.6	1.6
5	NMOS size (μm)	0.1	0.3	0.3	0.5	0.6	1.0	1.2	2.1	2.4	4.2	4.8	8.2	9.0	12.9	0.5
	PMOS size (μm)	0.1	0.4	1.0	1.7	1.9	3.3	3.9	6.7	7.8	13.3	15.5	26.2	28.7	41.3	1.6
6	NMOS size (μm)	0.0	0.2	0.2	0.4	0.5	0.8	0.9	1.6	1.9	3.3	3.8	6.5	7.1	10.8	0.5
	PMOS size (μm)	0.1	0.3	0.8	1.3	1.5	2.6	3.0	5.3	6.0	10.5	12.0	20.9	22.8	34.4	1.6
7	NMOS size (μm)	0.0	0.2	0.2	0.3	0.4	0.7	0.8	1.4	1.5	2.7	3.1	5.4	5.9	9.2	0.5
	PMOS size (μm)	0.0	0.3	0.6	1.1	1.2	2.2	2.5	4.4	4.9	8.7	9.8	17.3	18.8	29.5	1.6

Red cells show smaller values than the minimum size of transistors, thus the minimum size will be used for them.

(c)

Figure 2. (a) H-tree for timing signals. (b) Model for the route from Nth junction to (N+1)th junction. (c) Summary table of transistor sizes in various λ.

$C_{\rm in}$ is the input capacitance of the OR gate and $C_{\rm out}$ is its output load capacitance to drive the next stage including the input capacitance of the next OR gate [9]. λ at N_{th} junction is defined using the unit wire capacitance, C_w, as,

$$\lambda = C_{\rm out}/C_{\rm in} = (C_w \times 2^{({\rm int})(N/2)} + C_{{\rm in}(N+1)})/C_{{\rm in}(N)}. \tag{2.1}$$

The output of the H-tree is connected to unit size OR gate to minimize the input capacitance, so $C_{{\rm in}(13)}$ is a known value. Therefore, all $C_{\rm in}$ will be calculated successively. After all $C_{\rm in}$ are calcu-

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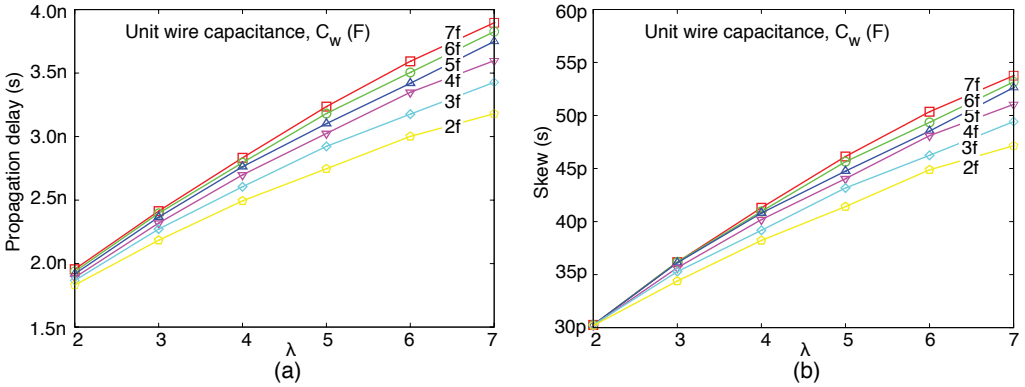

Figure 3. (a) Propagation delay and (b) skew in various λ values with different values of C_w.

lated, the transistor size of each OR gate is introduced as summarized in the table of figure 2 (c). Red cells show smaller values than the minimum size of transistors in our CMOS process, thus the minimum size will be used for them.

2.3 Simulation setup

A 2P4M high voltage 0.35 µm CMOS process is employed for our simulations. We set 0.35 µm and 0.5 µm as the minimum channel length and width of transistors, respectively. The simulator is Cadence Virtuoso Spectre Circuit Simulator, version 7.0.1.076.

3 Simulation results

3.1 Skew

Figure 3 and 4 show the propagation delay and skew for each λ varying C_w from 7 fF to 2 fF, and R_w, from 3.5 ohm to 1 ohm, respectively, assuming that each transistor channel length (L_{tr}), unit wire capacitance, and unit wire resistance has 5 % sigma process variation. Both the propagation delay and the skew improve dramatically by changing λ from 7 to 2 while the dissipated power increases 1.7 $\times$ and the transistor area increases 4.5 $\times$ at 7 fF C_w and 3.5 ohm R_w as shown in figure 5. One future option could be designing the D-SiPM using an advanced CMOS process, such as 180 nm, 130 nm or 90 nm to minimize the impact on fill factor. Note that C_w has more effect on the skew than R_w in the case of D-SiPMs, while R_w is very important for A-SiPMs [5]. The process variation for L_{tr}, C_w and R_w were set to vary from 5 % to 1% to see the dominant factor for the skew as shown in figure 6, thus demonstrating that L_{tr} has the highest impact on the skew.

3.2 Jitter

The temporal noise of the D-SiPM is composed of SPAD jitter, σ_{spad}, and noise due to timing signal routing, σ_{route}, including transistor induced noise and kTC noise [10]. The temporal noise model is shown in figure 7 (a). Figure 7 (b) shows the temporal noise by the timing signal routing. The temporal noise by the timing signal can be improved by employing a small value of λ due to small transition time. Assuming that all these sources of noise are wide-sense stationary (WSS), statistically independent random processes with Gaussian distribution (though the Gaussianity condition

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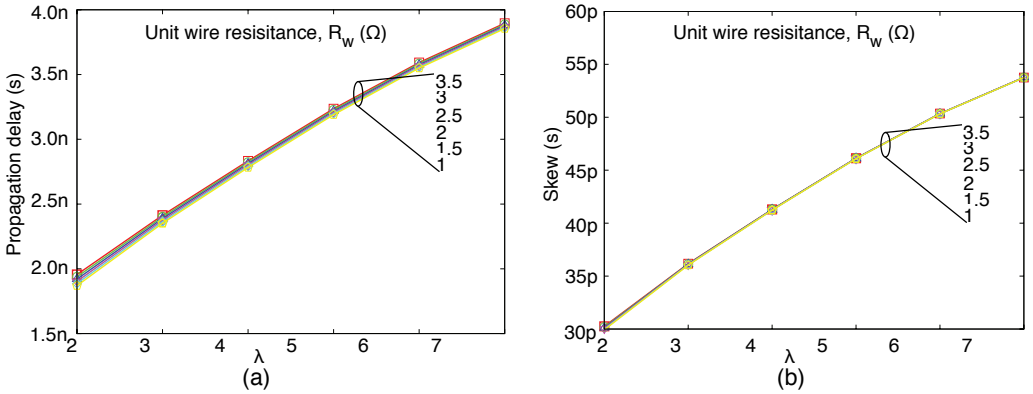

Figure 4. (a) Propagation delay and (b) skew in various λ with different values of R_w. R_w was found to have negligible effect on propagation delays and skews.

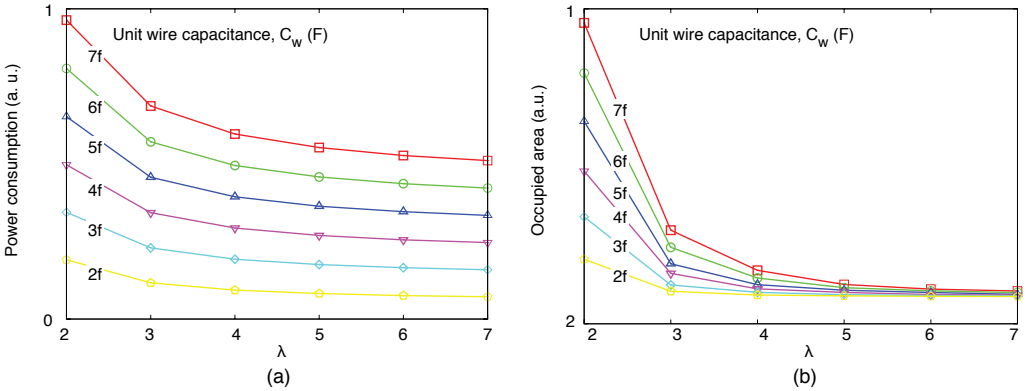

Figure 5. (a) Power consumption and (b) area occupation of H-tree drivers in various λ values.

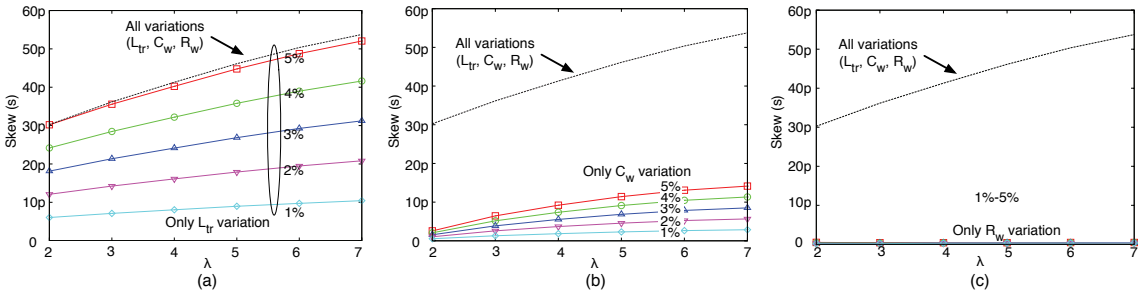

Figure 6. Skew dependency on (a) L_{tr}, (b) C_w and (c) R_w. For a broken line, the situation for which L_{tr}, C_w and R_w have 5% sigma process variation at the same time is considered as a reference.

may be relaxed if the WSS processes are identically distributed), the total standard deviation of the resulting process is computed as, $\sigma^2_{\text{jitter}} = \sigma^2_{\text{spad}} + \sigma^2_{\text{route}}$. Figure 7 (c) shows simulation results of the noise by routing, σ_{route}, and the total temporal noise, $\sigma_{\text{spad+route}}$, assuming that the SPAD jitter is 42.6 ps sigma [3]. It is observed that the SPAD jitter is dominant for the temporal jitter.

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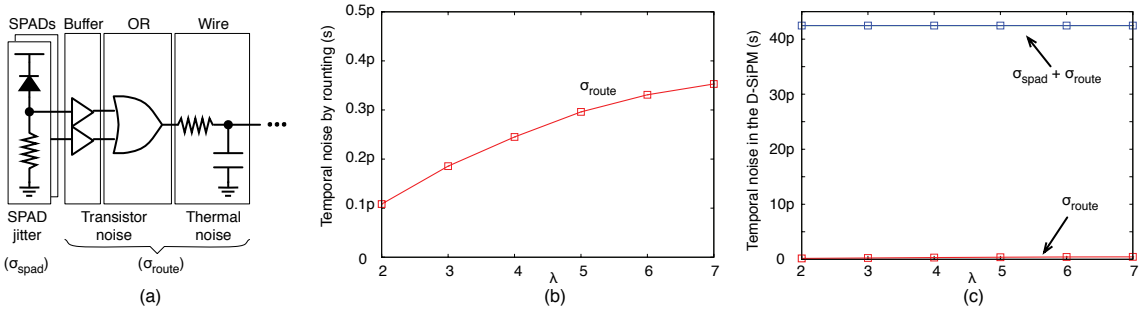

Figure 7. (a) Temporal noise sources in the D-SiPM. (b) Temporal noise by the timing signal routing. (c) Temporal noise in the D-SiPM in various values of λ.

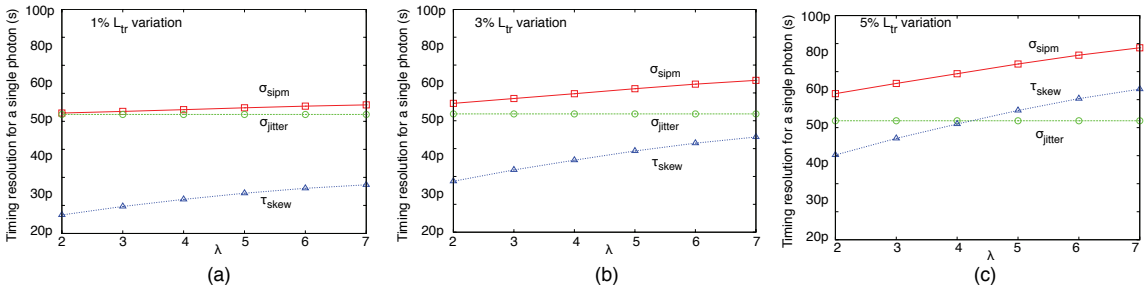

Figure 8. SPTR in sigma of a D-SiPM in each process variation; (a) 1%, (b) 2% and (c) 5%.

3.3 Single photon timing resolution (SPTR)

Under the same assumption of before, the SPTR of D-SiPMs is calculated as, $\sigma^2_{\text{sipm}} = \tau^2_{\text{skew}} + \sigma^2_{\text{jitter}}$. Figure 8 shows the SPTR of the D-SiPM for a range of λ derived from τ_{skew} and σ_{jitter} at 1, 3 and 5 % process variation. The timing resolution improves by utilizing small λ because the skew improves. In addition, the SPTR improves by reducing the transistor channel length variation and approaches to the SPAD jitter. We have also investigated the SPTR dependency on the size of the D-SiPM. Figure 9 (a) shows the timing resolution as a function of array size and λ. By reducing the size of the D-SiPM, the D-SiPM will be less sensitive to process variations because the skew becomes small. Therefore, to achieve good SPTR, the D-SiPM should be divided into small groups of SPADs, and connected to TDCs in another die with short 3-D vias, as shown in figure 9 (b), as well as optimizing the value of λ and designing transistors carefully not to have any geometrical asymmetry thus introducing L_{tr} variations.

3.4 Prediction of CTR in a PET application with a LYSO crystal scintillator.

To predict the CTR based on the SPTR computed in section 3.3 , we carried out another simulation, whereas the SPTF of the D-SiPM is swept from 10 ps to 100 ps in sigma while the parameters of a LYSO scintillator are the same as in [11]. Figure 10 (a) shows the relation between the SPTR and the predicted FWHM of CTR with various numbers of detected photons at negligible dark count rate (DCR) levels. According to the simulation results, the predicted CTR for the D-SiPMs can be improved from 221 ps to 190 ps and from 302 ps to 257 ps by improving the SPTR from 80 ps to 40 ps at 1000 and 500 primary photons, respectively, as shown in figure 10 (a). It means that

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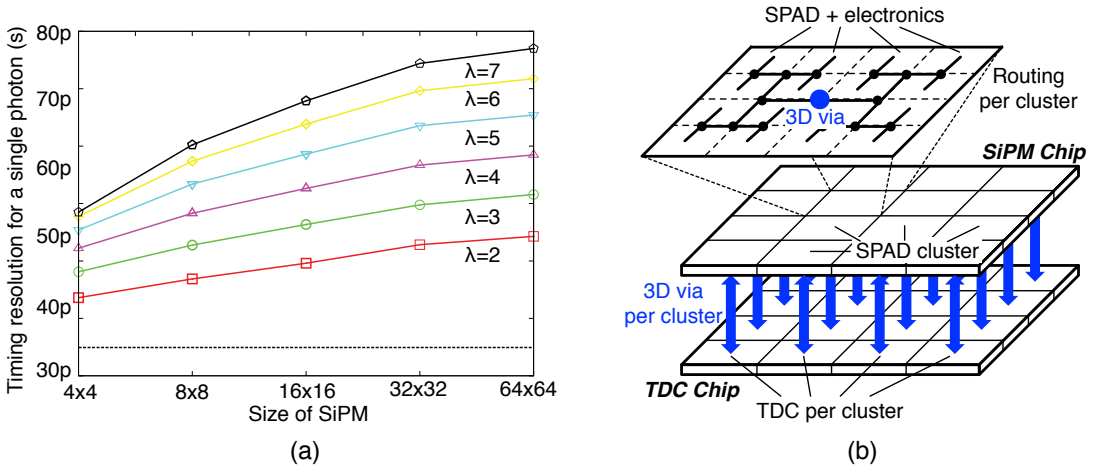

Figure 9. (a) SPTR in sigma of the D-SiPM in different sizes of array for the D-SiPM. (b) Ideal configuration of a D-SiPM implemented as a 3D IC.

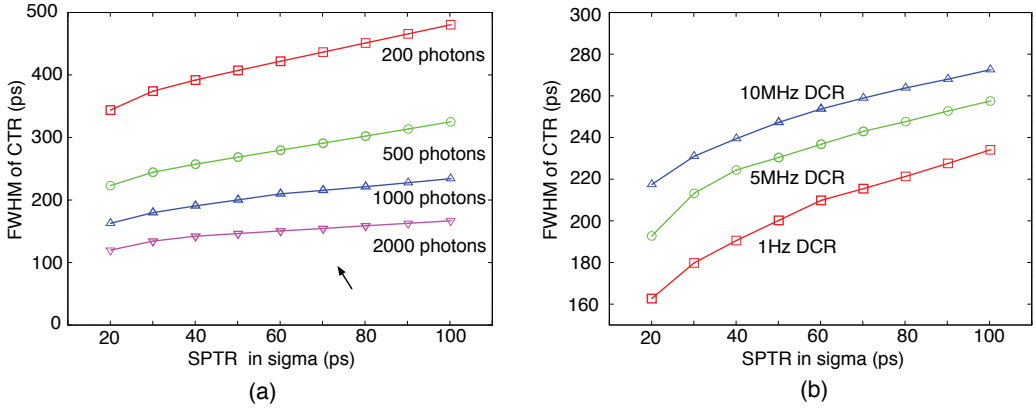

Figure 10. SPTR of a detector in sigma v.s. predicted FWHM of timing resolution (CTR): (a) various number of detected photons, 200, 500, 1000, and 2000 at 1 Hz DCR (which is almost negligible), (b) various values of DCR, 1 Hz, 5 MHz, 10 MHz at 1000 detected photons.

one can improve the CTR by changing the design parameter, λ, reducing the process variation of L_{tr}, C_w and R_w, or employing a SiPM divided to small groups of SPADs with individual TDCs as suggested in [3, 11]. This trend is also true for the different DCR as shown in figure 10 (b). Therefore, the D-SiPM architecture and these design parameters should be considered carefully following to one's target CTR in a PET application at the D-SiPM design stage.

4 Conclusion

We have presented the analysis of timing resolution for a D-SiPM using a SPICE simulator. Generally, a D-SiPM has more than a hundred of picoseconds timing resolution for single-photon detection due to detector jitter, circuit noise and routing skew. We found that SPAD jitter and skew have a strong impact on the timing resolution of the D-SiPM, though the timing resolution can be improved by choosing a proper architecture or modifying the design parameters: i.e. transistor

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width and length, wire resistance and capacitance, and their process variations. We have also shown the effect of these design parameters, as well as architectural choices, on the CTR of a PET, and demonstrated their strong impact on the CTR.

Acknowledgments

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