A 3.3-to-25V all-digital charge pump based system with temperature and load compensation for avalanche photodiode cameras with fixed sensitivity

2013 JINST 8 P03013

(http://iopscience.iop.org/1748-0221/8/03/P03013)

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *December 31, 2012*
ACCEPTED: *February 18, 2013*
PUBLISHED: *March 19, 2013*

2013 JINST 8 P03013

A 3.3-to-25V all-digital charge pump based system with temperature and load compensation for avalanche photodiode cameras with fixed sensitivity

S. Mandai[1] **and E. Charbon**

Faculty of Electrical Engineering, Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands

E-mail: s.mandai@tudelft.nl

ABSTRACT: This paper presents a digitally controlled charge pump (DCP) to supply high voltages, while ensuring temperature and load current independence of excess bias in cameras based on avalanche photodiodes. This is achieved through a single-photon avalanche diode (SPAD) based monitoring mechanism that continuously reconfigures the DCP using a feedback loop to compensate breakdown voltage variations by temperature and load current in real time. The sensitivity of the SPADs, or photon detection probability (PDP), is maintained to within 1.9% when the temperature shifts from 28°C to 65°C and the load current changes from 0 μA to 100 μA.

KEYWORDS: VLSI circuits; Analogue electronic circuits; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital electronic circuits

[1]Corresponding author.

doi:10.1088/1748-0221/8/03/P03013

Contents

2013 JINST 8 P03013

1 Introduction

Single-photon avalanche diodes (SPADs) are used as imaging devices in various fields, including molecular imaging, 3-D vision, space exploration, security monitoring, and biomedical diagnostics. SPADs need to be reverse-biased several volts above breakdown; these voltages are far beyond the transistor's operation conditions. Charge pumps based on the Dickson architecture are widely used to supply a high voltage proportional to the number of stages [1, 2]; these circuits are ideally suited for a SPAD biasing for bill-of-materials and cost reduction [3, 4]. Figure 1 shows the concept of a sensor based on a SPAD array with charge pump: each pixel consists of a SPAD, a current source, and ancillary circuitry. The cathode of the SPAD is biased to $V_{\mathrm{op}}, = V_{\mathrm{bd}} + V_{\mathrm{e}}$, where V_{bd} is the breakdown voltage and V_{e} the excess bias. The anode, V_{pix}, is connected to an active quenching circuit used to stop an avalanche quickly enough to prevent device destruction with a long enough hold-up time to enable detection. During the detection cycle, V_{pix} reaches V_{e} in less than 1 ns and returns to ground absorbing a current pulse $I_{\mathrm{source}}(t)$, upon a photon or thermal event. The width of the pulse is proportional to V_{e} and the sum of all impulsive currents, I_{sum}, is proportional to the illumination brightness and must thus be guaranteed by the voltage generator under all specified lighting conditions. In addition, the generator must also adjust V_{op} to maintain a constant excess bias when the breakdown voltage changes, due to process and temperature variations and

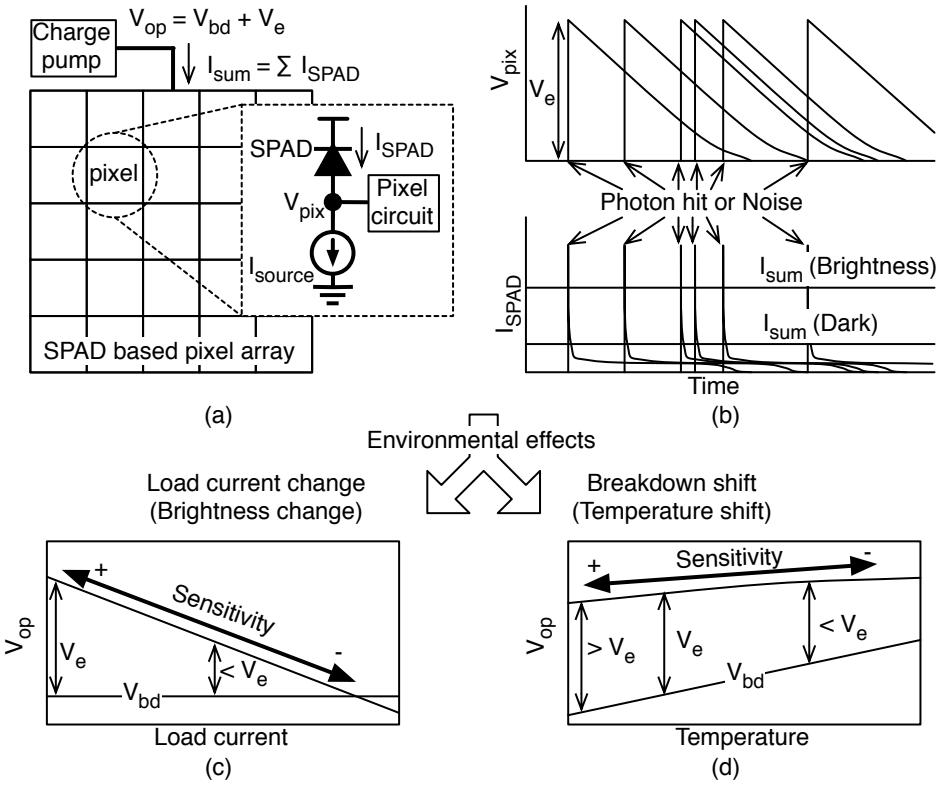


Figure 1. (a) Concept of a SPAD array with excess bias voltage stabilization via charge pump. (b) Superimposed oscilloscope traces of pixel responses. (c),(d) Typical response of conventional charge pump output as a function of load current and temperature with respect to breakdown voltage V_{bd}. Sensitivity varies with excess bias and thus it will degrade with an increase temperature and load current, if measures are not taken.

to account for current absorption variations at V_{op} due to increase of brightness [3, 4]. The charge pump proposed in [5] is insensitive to current variations but still the charge pump is sensitive to temperature fluctuation. Thus maintaining the excess bias irrespective of process, voltage, temperature, and brightness (PVT-B) variations is essential to ensure constant and reliable sensitivity levels of SPAD arrays over long periods of time, as demanded by today's applications.

This paper presents a digitally controlled charge pump (DCP) based system to supply high voltages, while assuring PVT-B independence of excess bias in large SPAD arrays. This is achieved through a SPAD-based environment monitoring mechanism that continuously reconfigures the DCP using a feedback loop to compensate for temperature and breakdown voltage variations in real time. The sensitivity of the SPADs, or photon detection probability (PDP), is maintained to within 1.9% when the temperature shifts from 28°C to 65°C and the load current changes from 0 to 100 μA.

The paper is organized as follows. Section 2 shows the architecture and circuit implementation. Section 3 presents each component's characterization and section 4 demonstrates the system operation. Finally, conclusions are given in section 5.

2013 JINST 8 P03013

2 Architecture and implementation

2.1 System architecture

Excess bias is estimated utilizing dark count rate (DCR) and the pulse width of SPAD output. DCR is a function of the temperature and excess bias, being shown as $DCR = f(T, V_e)$ using temperature, T, and excess bias V_e. The pulse width, PW, is calculated using the SPAD capacitance, C_{spad}, and current source, I_{source} assuming that the parasitic capacitances of the peripheral circuit of SPADs are small, as shown, $PW = V_e \times C(T)/I_{source}(T)$. Therefore, excess bias is the solution of the simultaneous equation shown below,

$$DCR = f(T, V_e) \tag{2.1}$$

$$PW = g(T, V_e) \tag{2.2}$$

In this system, after estimating the excess bias by observing DCR and pulse width using a DCR counter and a pulse-width-to-digital converter (PWDC), DCP is reconfigured according to the estimation to keep the excess bias constant. This procedure will be iterated in real time to adapt a dynamic environment change.

2.2 Digitally controlled charge pump

Figure 2 shows the schematic of the DCP; it is clocked by a 6-bit digital controlled oscillator (DCO), whose frequency can be swept from 43.7 MHz to 1.2 GHz. The DCP resembles a 11-stage Dickson architecture, except for a parasitic capacitance, $C_{parasitic}$, in each stage that can be digitally modulated via NMOS switches. The voltage gain in each stage is $(V_{dd} - V_t)C/(C_{parasitic} + C)$, where V_{dd} is the power supply, V_t the threshold voltage of the stage's diode, and C, the main capacitance. The input voltage of the DCP is 3.3 V, the nominal power supply voltage, and C is 1.64 pF. The DCP output voltage modulation step is approximately 80 mV and it depends on the DCP frequency and I_{sum}. This voltage step was chosen as 1% of the detector sensitivity.

2.3 Environment monitor

Figure 3 shows a schematic of the environment monitor. The monitor acquires the dark counts and computes the dark count rate (DCR) of a reference SPAD that was shielded from light; it also measures the width of the avalanche pulses of the SPAD. The width of the avalanche pulse is proportional to the excess bias, the SPAD capacitance and a FPGA-controlled capacitance. The latter is used to enlarge the avalanche pulse, which looks like a sawtooth, to make it easier to measure its width. The avalanche pulse is converted onto a square wave, EN, by a comparator and digitized to a digital code with the PWDC. The PWDC consists of 4-stage differential inverter chain with a 10-bit counter; the inverter chain oscillates when EN in on. The frequency of oscillation is the inverse of the timing resolution, which in turn is dynamically checked by the replica PWDC that is fed a reference pulse generated by a temperature independent PLL on a FPGA. The DCR and avalanche pulse width will be used to estimate the temperature and the excess bias of the SPAD. There are three identical environment monitors operating in parallel to increase the estimation speed and to cope with low DCR.

2013 JINST 8 P03013

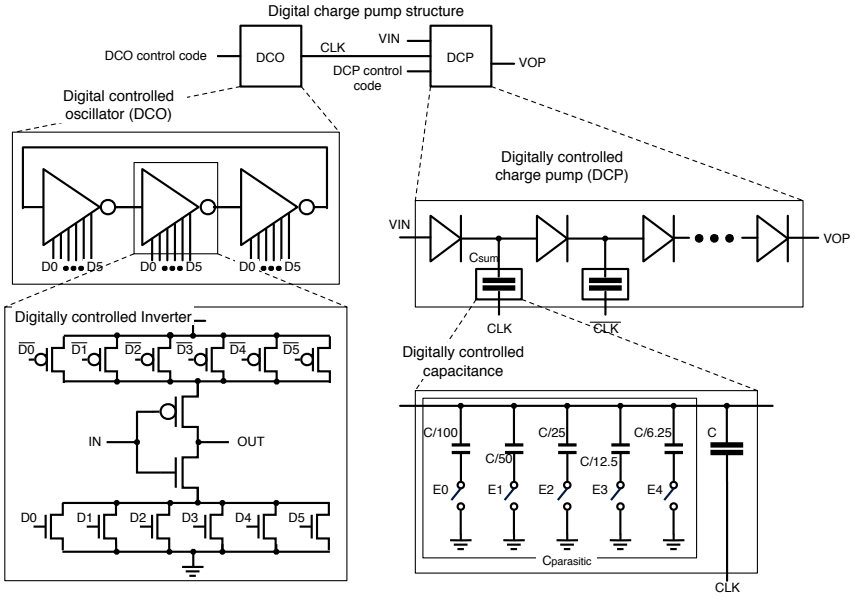


Figure 2. Block diagram of the digitally controlled charge pump and schematics of its components. DCO is a three-stage digitally controlled ring oscillator by changing the number of current sources. DCP is also digitally controlled to change the ratio of the peripheral capacitance by NMOS switches.

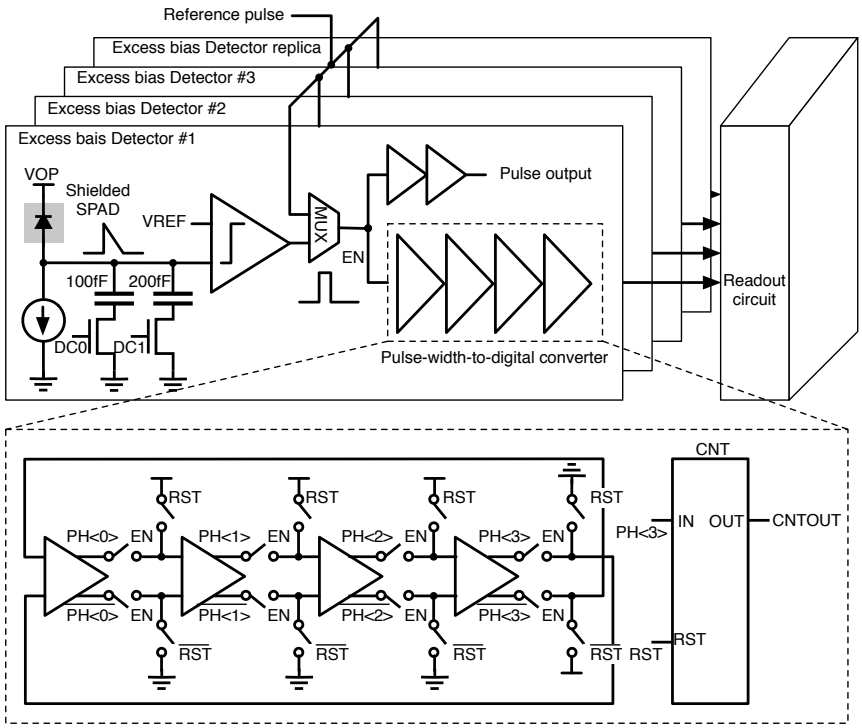


Figure 3. Schematic of the environment monitor, comprising an array of shielded SPADs, a comparator, the pulse-width-to-digital converter, and readout circuitry.

2013 JINST 8 P03013

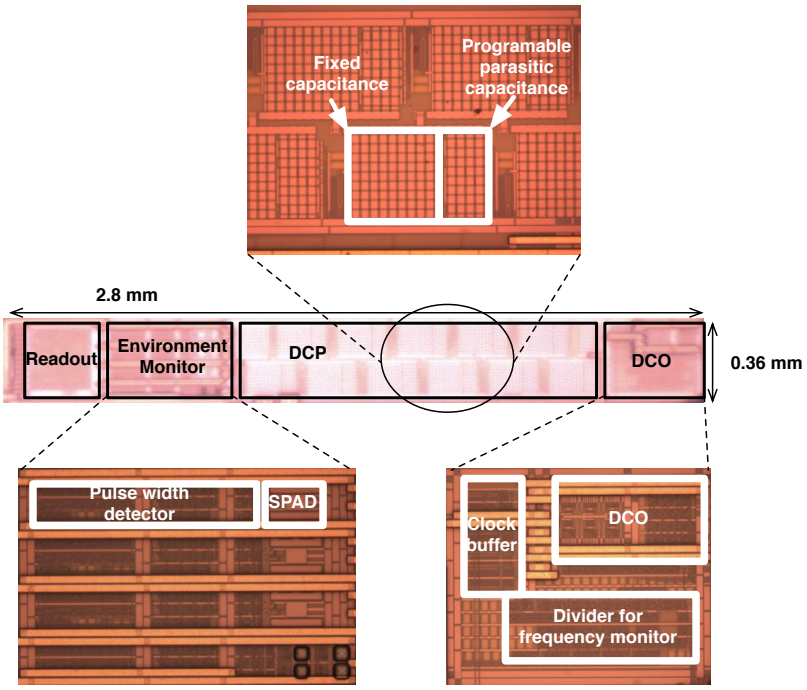


Figure 4. Chip microphotograph. Details of the circuit are shown in the insets. The chip measures $2.8 \times 0.36\,\mathrm{mm}^2$ and it was fabricated in a commercial $0.35\,\mu$m CMOS process.

3 DCP and environment monitor characterization

3.1 Chip fabrication

The DCP and the environment monitor have been designed and fabricated using a 2P4M high voltage $0.35\,\mu$m CMOS process. A photomicrograph of the chip is shown in figure 4. The figure shows the die size is $0.36 \times 2.7\,\mathrm{mm}^2$. The $6\,\mu$m diameter SPAD comprises a p+ / deep n-well junction with a p-well guard ring [6]. The breakdown voltage at 20°C is 19.6 V. The quenching current source generates $15\,\mu$A.

3.2 DCP characterization

The DCP was characterized first in open-loop and subsequently in closed-loop, with a controlled load current and temperature. Figure 5 (a) shows the DCP output voltage plotted as a function of DCO clock frequency and control coding in an open-loop operation mode. DCO and DCP control code are corresponding to D5-D0 and E4-E0 in figure 2. DCO frequency is swept with 720 ns step and the DCP output voltage becomes stable within 720 ns. Figure 5 (b) shows the DCP output voltage as a function of clock frequency for selected codes; one can see that the maximum voltage is achieved at one optimal clock frequency. Figure 5 (c) shows that the optimal frequency shifts up by increasing loading for a given control code, while figure 5 (d) shows how the DCP output voltage varies with different control codes by changing the loading, when the DCP is operated at the optimal clock frequency for that loading level.

2013 JINST 8 P03013

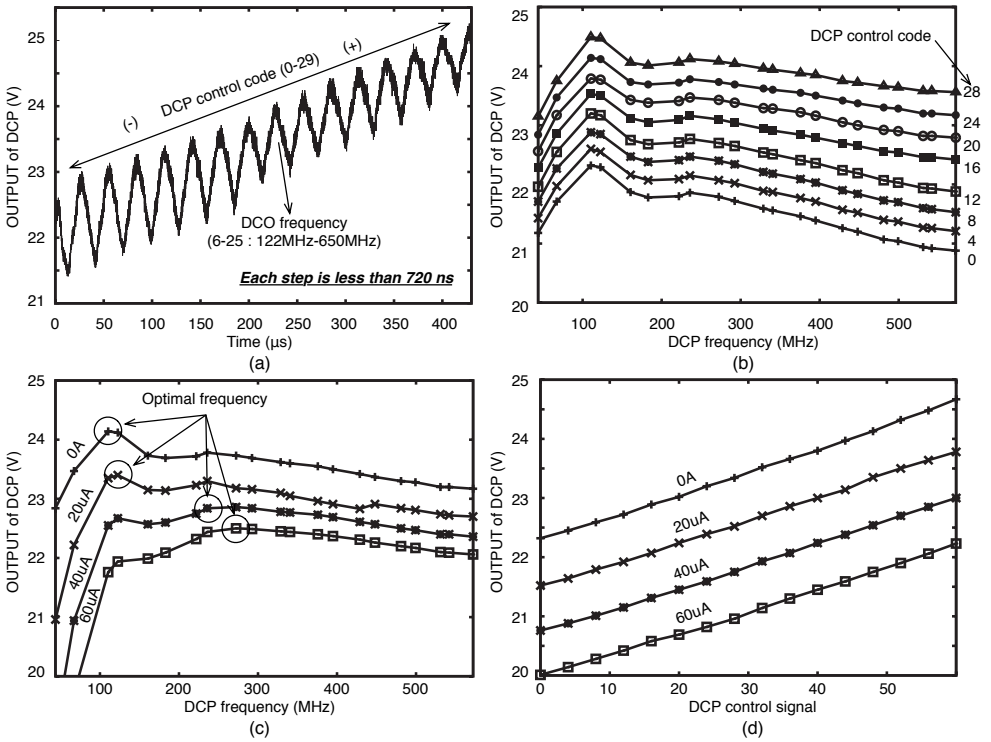


Figure 5. Measurement results of the digitally controlled charge pump (DCP). (a) Transient sweeping of the DCO clock frequency and DCP control code. (b) DCP output voltage as a function of DCO frequency and DCP control code. (c), (d) DCP output voltage as a function of DCO frequency for a given DCP code at various loading levels.

3.3 Environmental monitor characterization

The resolution of PWDC is 204 ps at 20°C , and has a INL of +0.5 / -1.6 LSB in 1.24 μs input range; note that the typical single-shot jitter is 1.6 LSB (FWHM). The resolution improves by 4.1 ps and 4.3 ps by cooling the device to 10°C and by increasing the power supply voltage by 0.1 V, respectively. Figure 6 (a) plots the pulse width histogram of SPAD avalanche pulses occurred in 153 seconds and measured by the PWDC at several excess bias values from 1.5 V to 3.5 V with a 0.5 V step, spanning a temperature range from 0°C to 70°C with a 10°C step. The average FWHM of the pulse width is 13.8 ns, corresponding to 115 mV of excess bias and 21.6°C temperature resolution. By averaging the results over 200 iterations, the FWHM can be improved to 3.47 ns, corresponding to 28.9 mV of excess bias and 5.4°C temperature resolution. The estimation time is limited by DCR, the DCR being less than 10 Hz at lower temperatures. Figure 6 (b) summarizes the relation between DCR and pulse width at various temperature and excess bias combinations. By utilizing a DCR and pulse width map, intermediate temperature and excess bias values can be accurately estimated by way of interpolation. Figure 6 (c) summarizes the relations between pulse width, DCR, temperature, and excess bias.

2013 JINST 8 P03013

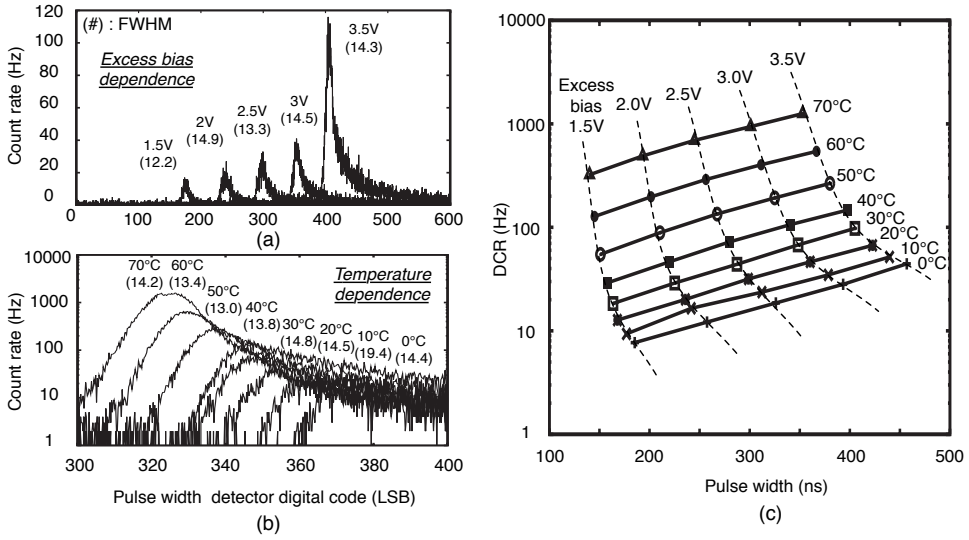


Figure 6. Estimation of avalanche pulse width and excess bias in various environmental conditions. (a) Pulse width histograms as a function of excess biases and temperature; in parentheses the FWHM jitter of the measurement. (b) Pulse width histograms as a function of DCR for various temperatures; note that low DCRs result in worse width estimation uncertainties, shown in parentheses. (c) Pulse width estimation vs. DCR for various combinations of excess bias and temperature.

4 System operation

4.1 System setup

The DCP was tested in closed-loop configuration, whereas the environment monitor is used in the feedback. Figure 7 (a) shows the block diagram for the feedback loop. The SPAD array is emulated by a variable current source. The DCP output is provided to three SPAD cathodes. All SPAD outputs are read out and monitored by FPGA, simultaneously, the SPAD outputs are rectified and converted to digital codes by a bank of PWDCs. The DCR calculator counts the count rate and the Pulse width calculator takes averages of the pulse width. The PWDC is dynamically calibrated using a replica pulse from a temperature-insensitive PLL in the FPGA. FPGA and host PC estimate the excess bias of the SPADs using a look-up table (LUT) which has been pre-calculated during a calibration phase. Based on the estimation, the proper digital code for DCP and DCO is generated and available from the FPGA. Figure 7 (b) shows the timing diagram of the system. The system clock frequency is 20 MHz. After reset, the replica pulse is generated. Once one of the SPADs fires, the FPGA starts to read out the latched data of all PWDCs in 26 clock cycles. Then, the system again waits until the next dark count occurs in an event driven scheme.

4.2 Interpolation method for excess bias and temperature information

Figure 8 shows the excess bias and temperature information estimation based on LUT acquired beforehand. To acquire excess bias and temperature information based on interpolation method, the parameter, α and β should be solved using measured vector $\vec{x}$, and temperature direction, and

2013 JINST 8 P03013

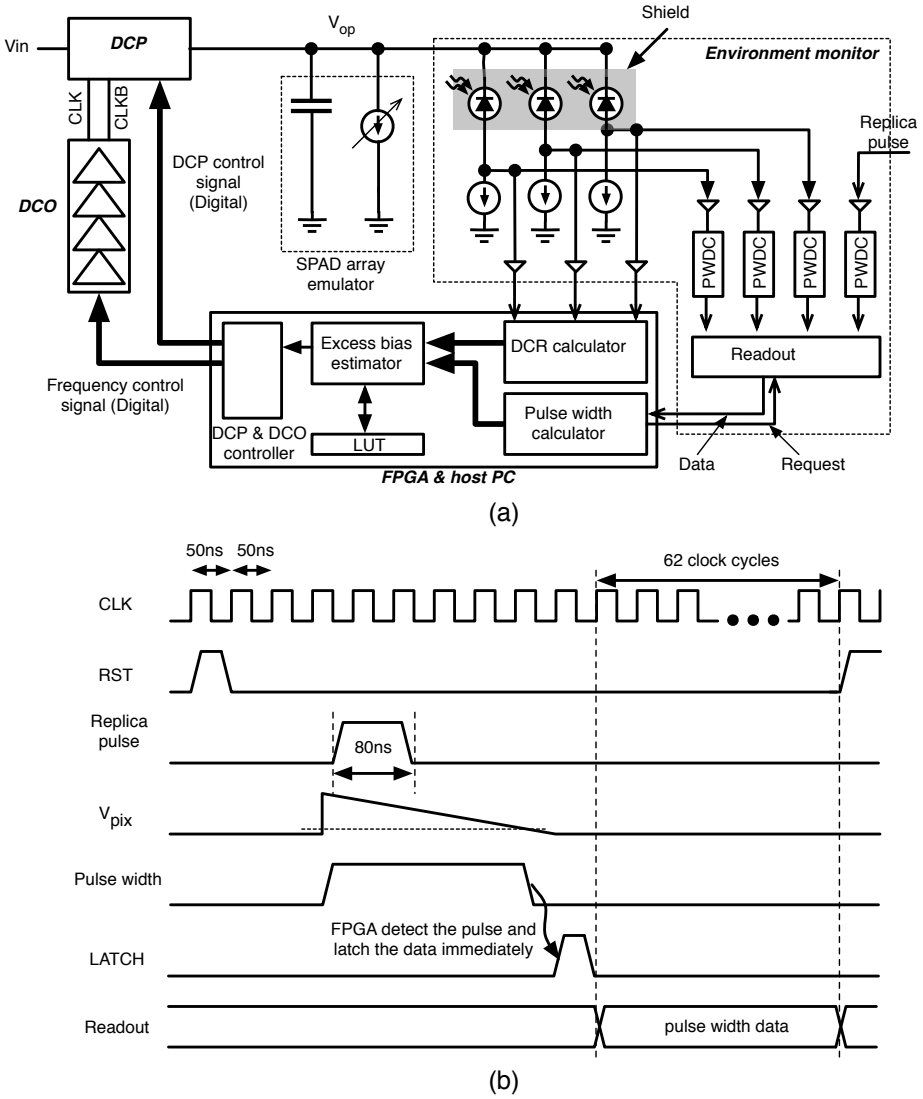


Figure 7. Feedback operation detail and extra measurement results. (a) Block diagram for the feedback loop. (b) Timing diagram. The readout circuit starts to read out as soon as the FPGA detects the DCR pulse. The minimum number of clock cycles to read out the data from three PWDCs and the replica PWDC, is 62.

excess bias direction vector, $\vec{a}$ and $\vec{b}$, from the equations shown below,

$$\vec{x} = \alpha\vec{a} + \beta\vec{b}.$$

By assuming that $\vec{a} = (\Delta PW_a, \Delta DCR_a)$, $\vec{b} = (\Delta PW_b, \Delta DCR_b)$ and $\vec{x} = (\Delta PW_x, \Delta DCR_x)$, α and β can be calculated as below,

$$\alpha = \frac{DCR_b PW_x - PW_b DCR_x}{PW_a DCR_b - PW_b DCR_a} \tag{4.1}$$

$$\beta = \frac{DCR_a PW_x - PW_a DCR_x}{PW_b DCR_a - PW_a DCR_b} \tag{4.2}$$

2013 JINST 8 P03013

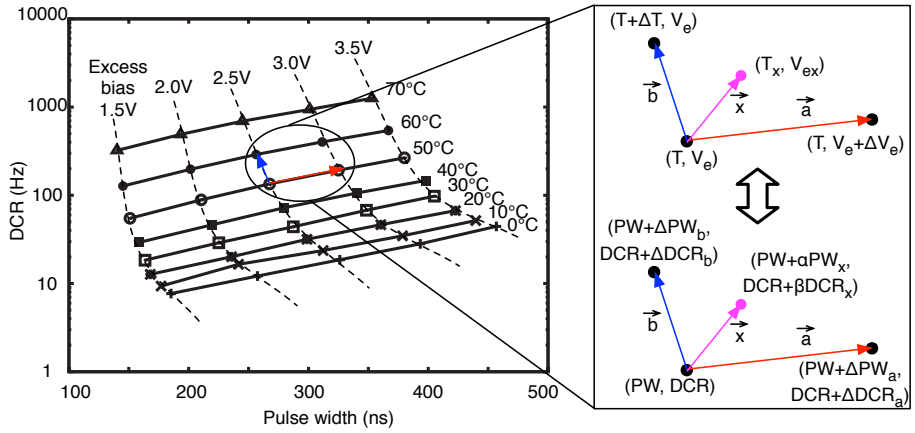


Figure 8. Interpolation method to acquire excess bias and temperature information using coarse calibration data.

Then current excess bias, V_{ex}, and current temperature, T_x, are calculated using excess bias step, ΔV_e, and temperature step, ΔT, based on the course calibration beforehand (figure 6 (c) and figure 8) as below

$$V_{ex} = V_e + \alpha \times \Delta V_e \tag{4.3}$$

$$T_x = T + \beta \times \Delta T \tag{4.4}$$

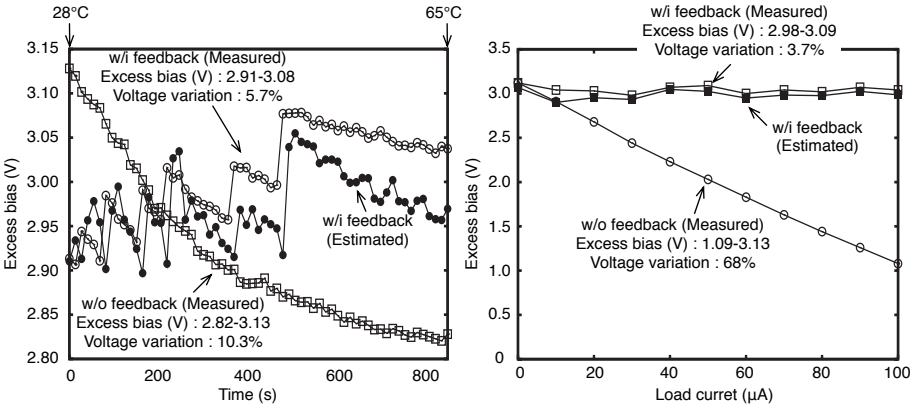
4.3 System characterization

Figure 9 (a) and (b) show the measured excess bias with and without feedback. The excess bias is reconfigured in real time when temperature or load current are dynamically changed with the feedback loop described above. The resulting estimated excess bias derived from the LUT is also drawn in the same graph. The average excess bias difference between measurement and estimation is 78 mV and 60 mV for the temperature and the load current sweep, respectively. A voltage variation of 5.7% and 3.7% were measured with feedback when the temperature ranged from 28°C to 65°C and the load current from 0 A to 100 μA, respectively versus a 10.3% and 68% variation without feedback. With feedback the variation in sensitivity was only 1.9% at a wavelength of 450 nm in the entire temperature range. Figure 9 (c) summarizes the features of the proposed high-voltage generator and compares it with the literature [2, 3, 5].

5 Conclusion

We have presented a digitally controlled charge pump (DCP) to supply high voltages, while ensuring temperature and load current independence of excess bias in cameras based on avalanche photodiodes. This is achieved through a single-photon avalanche diode (SPAD) based monitoring mechanism that continuously reconfigures the DCP using a feedback loop to compensate breakdown voltage variations by temperature and load current in real time. The sensitivity of the SPADs, or photon detection probability (PDP), is maintained to within 1.9% when the temperature shifts from 28°C to 65°C and the load current changes from 0 μA to 100 μA.

2013 JINST 8 P03013



Features	This work	[2]	[3]	[5]
Technology	350 nm	130nm	90nm	180nm
Area	0.36 mm x 2.8 mm	0.3 mm x 0.1 mm	0.12 mm x 0.16 mm	2.05 mm x 1.95 mm
Output voltage	21.4 V - 25 V	1.2 V to 8V	10.9 V	1.2 V - 6 V
Application	SPAD based camera	Non-volatile memory	SPAD based camera	Earphone
Current change	**Insensitive**	Sensitive	Sensitive	**Insensitive**
Temperature shift	**Insensitive**	Sensitive	Sensitive	Sensitive

(c)

Figure 9. Excess bias voltage control results with and without feedback (a) as a function of temperature and (b) load current. (c) Specification summary and comparison with literature.

Acknowledgments

The authors would like to thank Dr. M.W. Fishburn of TU Delft for many useful discussions.

References

[1] J.F. Dickson, *On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique*, *IEEE J. Solid State Circ.* **11** (1976) 374.

[2] A. Richelli, L. Mensi, L. Colalongo, P.L. Rolandi and Z.M. Kovacs-Vajna, *A 1.2-to-8V Charge-Pump with Improved Power Efficiency for Non-Volatile Memories*, *IEEE Solid State Circ. Conf.* **2007** (2007) 552.

[3] R.K. Henderson, E.A.G. Webster, R. Walker, J.A. Richardson and L.A. Grant, *A* 3×3*,* $5\,\mu m$ *pitch, 3-transistor Single Photon Avalanche Diode Array with Integrated 11V Bias Generation in* $90\,nm$ *CMOS Technology*, *IEEE Int. Electron Dev. Meeting* **2010** (2010) 14.2.1.

[4] M. Al-Rawhani, D. Cumming, D. Chitnis and S. Collins, *Photocurrent Dependent Response of a SPAD biased by a charge pump*, *IEEE Int. Symp. Sirc. Syst. ISCAS* **2009** (2011) 789.

[5] C.Y. Tseng, S.C. Chen, T.K. Shia and P.C. Huang, *An Integrated 1.2V-to-6V CMOS Charge-Pump for Electret Earphone*, *IEEE Symp. VLSI Circ.* **2007** (2007) 102.

[6] C. Niclass, C. Favi, T. Kluter, M.A. Gersbach and E. Charbon, *A* 128×128 *single-photon image sensor with column-level 10-bit time-to- digital converter array*, *IEEE J. Solid State Circ.* **43** (2008) 2977.

2013 JINST 8 P03013