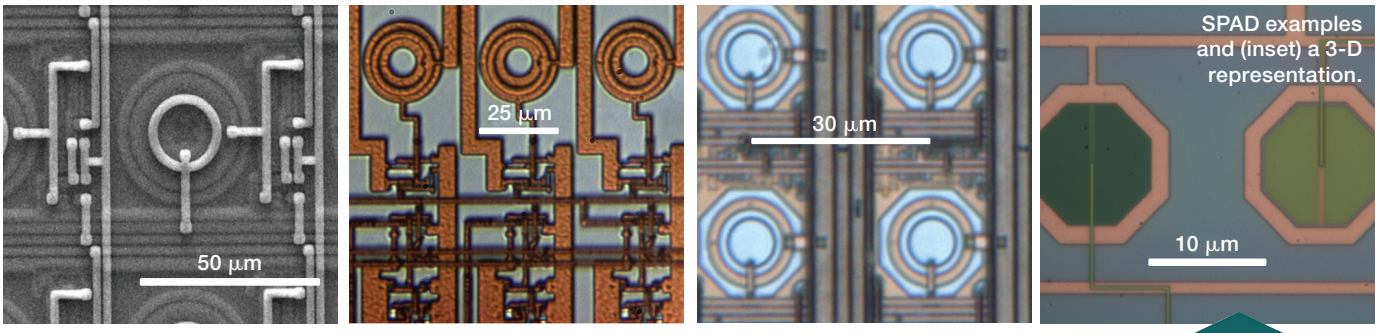
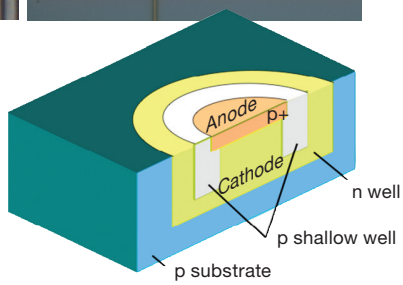


Evolving CMOS Technology for High-Performance

Single-Photon Detection



Edoardo Charbon

For decades, solid-state detectors could detect individual photons. This is now possible to do using avalanche photodiodes. So-called single-photon avalanche diodes (SPADs) are biased above breakdown in Geiger mode and fabricated using CMOS processes.

The primary engineering challenge of SPAD fabrication is figuring out how to prevent premature edge breakdown at the sharp edges of implant boundaries, where the electric field is high. Proper doping can reduce this field, but doped regions must be carefully designed to prevent depletion regions that extend too far under the active region with high bias voltages, and to avoid doping differentials that are too small to prevent edge breakdown.

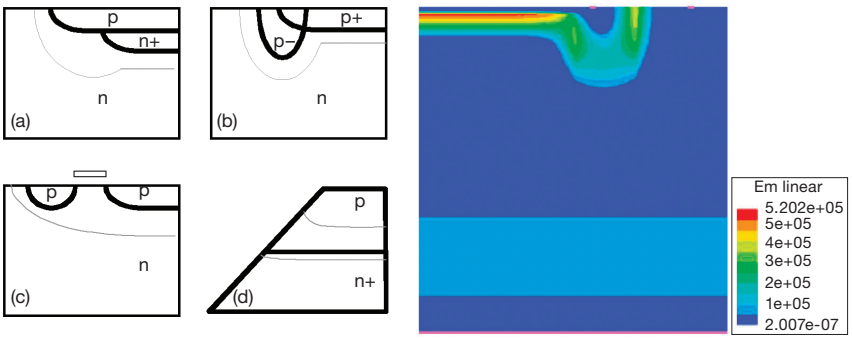
Standardized CMOS processes limit available doping profiles, but performance can be recovered with clever layout and digital signal processing. Well-established CMOS techniques reduce the electric field at edges and everywhere else in the device, thereby maximizing the probability that avalanche initiates in the center of the multiplication region, where the critical electric field for impact ionization is achieved. Deep knowledge of the mechanisms underlying impact ionization and avalanching is critial to success.

The figure to the right shows common structures of CMOS SPADs. In (a), the n+ layer maximizes the electric field in the center of the diode. In (b), the lightly doped p-implant reduces the electric field at the edge of the p+ implant. In (c), a floating p-type implant locally increases the breakdown voltage. With a polysilicon gate, the depletion region (gray line) is extended further. Scheme (d) decreases the electric field using shallow and/or deep trenches. However, traps may form in trenches, and they are deleterious to SPAD performance because they may cause carrier generation beneath high voltage regimes and trigger spurious avalanches. Traps can be prevented by stacking layers with decreasing doping levels from the trench to the multiplication region. Short mean-free paths are achieved near the trench, forcing generated carriers to recombine.

Methodologies for optimization: The SPAD farm

Designing a novel CMOS SPAD requires several iterations, in which the engineer

[Common structures of CMOS SPADs]



(Left) Premature edge breakdown prevention mechanisms in planar and semi-planar processes. (Right) A simulation of the electric field distribution around the guard ring of style (b). Note that the electric field is maximized in the anodic region and kept below the critical level for impact ionization in silicon on the guard ring.

must compare arrays of new and current test structures. Specific parameters (typically three) are systematically varied to achieve an optimal combination. This test structure array is called a SPAD farm. Several steps test a SPAD farm, including variation of process, supply voltage and temperature. Promising structures are integrated with quenching and decoupling electronics to test their dynamic and saturation properties. Iterative optimization can continue for years.

An example optimization involves the dark count rate—i.e., noise due to band-to-band tunneling that is dependent on doping profiles near the multiplication region. Low doping levels extend the depletion region, creating ohmic contacts that prevent proper biasing to achieve Geiger mode operation.

SPAD fabrication challenges continue beyond the SPAD farm. The quenching and recharge mechanisms must be designed with identical technology. Quenching circuitries stop the avalanche, thereby preventing device destruction. Recharge circuitries prepare the SPAD for the next detection cycle by raising the bias voltage back to its initial state. Quenching and recharge can be active or passive. In active mode, active circuitries control the process. In passive mode, the avalanche current passively controls the process by way of a ballast resistive device.

Active quenching and recharge allow for better control of the detection cycle and the overall time spent quenching and recharging, which is known as dead time. This important parameter determines the detector's maximum count rate and saturation flux. A variety of active quenching and recharge circuits are in the literature. Options can be complex, allowing for dead time programmability and stability. However, when miniaturization is important, simplicity of the recharge mechanism is paramount.

> Designing a novel CMOS SPAD requires several iterations, in which the engineer must compare arrays of new and current test structures.

SPAD characterization

The table below shows the parameters used to characterize SPADs for four different CMOS processes. Spectral sensitivity is measured as photon detection probability, which is the probability that a photon successfully generates a digital pulse. Noise performance is measured as the rate of spurious pulses due to thermal events—the dark count rate; it varies from Hz to MHz. Timing jitter (or resolution) is the uncertainty between actual and measured photon arrival time, ranging from tens of picoseconds to nanoseconds. After-pulsing probability is the probability that an avalanche causes spurious avalanches; it is measured as a fraction of the dead time.

[Comparison of CMOS SPAD performance for a variety of devices]

Measurement	0.8 μm CMOS	0.35 μm CMOS	130 μm CMOS	130 μm CMOS
Timing jitter (FWHM @ 637nm)	82 ps	80 ps	125 ps	200 ps
DCR (mean at 300K)	350 (V_E: 5.0V) Hz	750 (V_E: 3.3V) Hz	220 (V_E: 2.0V) Hz	1221 (V_E: 0.6V) Hz
Active area	38 μm^2	78 μm^2	58 μm^2	50 μm^2
Mean DCR per active area	9.2 Hz/μm^2	.6 Hz/μm^2	3.8 Hz/μm^2	24.4 Hz/μm^2
Breakdown (VBD)	25.5 V	17.4 V	12.8 V	14.4 V
Dead time	<40 ns	40 ns	100 ns	100 ns
PDP @ 460nm	26 (V_E: 5.0V)%	40 (V_E: 3.3V)%	26 (V_E: 2.0V)%	17.5 (V_E: 0.6V)%
Spectral range (PDP > 1%)	380~900 nm	350~1000 nm	380~900 nm	350~1000 nm

When implemented in an imaging array, uniformity of the aforementioned parameters must be properly characterized. These parameters are a function of excess bias voltage, temperature and wavelength.

An important imaging array parameter is crosstalk, which may be electrical and optical. Electrical crosstalk occurs for conventional pixels, while optical crosstalk is specific to SPADs. Optical crosstalk may occur when an avalanche is triggered in an aggressor pixel. By impact ionization, several photons may be emitted, causing a victim pixel to detect them. Electrical crosstalk is dependent on the supply line design and substrate noise rejection techniques, but optical crosstalk may only be influenced by the number of carriers involved in an avalanche and by pixel pitch. Reducing the avalanching carriers is best achieved by reducing the active area of a SPAD, and thus its capacitance, leading to a lower fill factor for a constant pixel pitch. With these advances using CMOS technologies, it is now possible to envision large imaging arrays based on SPADs.

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