

Characterization of Large-Scale Non-Uniformities in a 20k TDC/SPAD Array Integrated in a 130nm CMOS Process

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Abstract—With the emergence of large arrays of high-functionality pixels, it has become critical to characterize the performance non-uniformity of such arrays. In this paper we characterize a 160x128 array of complex pixels, each with a single-photon avalanche diode (SPAD) and a time-to-digital converter (TDC). A study of the array's non-uniformities in terms of the timing resolution, jitter, and photon responsivity is conducted for the pixels at various illumination levels, temperatures, and other operating conditions. In the study we found that, in photon-starved operation, the TDCs exhibit a median resolution of 55ps and a standard deviation of 2 ps. The pixels show a median timing jitter of 140ps. Moreover, we measured negligible variations in photon responsivity while changing the number of active pixels. These findings suggest that the image sensor can be used in highly reliable, large-scale, time-correlated measurements of single photons for biological, molecular, and medical applications. The chip is especially valuable for time-resolved imaging, single-photon counting, and correlation-spectroscopy under many realistic operating conditions.

I. INTRODUCTION

Time-resolved imaging has proven its potential to various applications ranging from machine vision to microscopy. Applications such as Fluorescence lifetime imaging microscopy (FLIM), Forster resonance energy transfer (FRET), optical range finding, and fluorescence correlation spectroscopy (FCS) have created a need for a wide-field, low-cost, single-photon, time-resolved imager. The general trend in imaging technology is to reach a picosecond time resolution with millions of measurements per second and an increasing image resolution. Photomultiplier tubes are capable of picosecond resolutions over relatively large sensitive areas, but lack imaging capability that is usually achieved via optical scanning. Multi-channel plates provide such capability, but are still relatively bulky and costly. Solid state single photon avalanche diodes (SPADs) [1] are increasingly adopted as a good compromise between cost and performance, especially after multi-pixel CMOS SPAD imagers have appeared [2] [3] [4]. The integration of single-photon avalanche diodes in deep submicron CMOS technology has led to the development of low-cost, single-photon, time-resolved, pixelated arrays of image sensors.

As SPAD array sizes have grown, the on-chip readout bottleneck has also become evident, leading to complex technological solutions [5] and more parallelism on-chip [6]. This trend has enabled the design of massively parallel arrays with the entire photon detection and time-of-arrival (TOA) circuitry being integrated on-pixel [7] [8] [9] [10], and thus enabling real-time FLIM [11]. The integration of complex pixel arrays with on-pixel photon detection and TOA circuitry has led to a need to understand the effect on the performance of the photon detection capability of the pixel and on its timing sensitivity with respect to standalone devices. This work presents the largest ever devised SPAD-based imagers [10], studied for its performance uniformity in terms of photon sensitivity and timing performance.

The presented chip [10] is an imager with 160x128 pixels capable of measuring the time-of-arrival of single photons. Every pixel in this imager is made of a single-photon avalanche diode and a 10b, ring-oscillator-based time-to-digital converter (TDC). The 10b data generated by every pixel is read out using two sets of serializers available at either end of the imager, one serializer per half-column. This image sensor is designed to work in two different modes of operation, time-uncorrelated photon counting (TUPC) mode and time correlated single photon counting (TCSPC) mode. In TUPC mode the sensor counts the number of photon arrivals in a period of time, whereas in time-correlated mode the arrival time of every detected photon is measured with respect to a time reference. Section II presents characterization results for TUPC mode, and Section III presents results for TCSPC mode and uniformity of pixel timing performance. Section IV presents concluding remarks and a discussion.

II. TIME-UNCORRELATED PHOTON COUNTING MODE

In TUPC mode, the measured photon count in a SPAD-based imager is a function of several intrinsic factors, including the pixel fill factor, the photon detection probability (PDP) and the dark count rate (DCR) of the SPAD. In this paper photon detection uniformity across the array is analyzed

based on the variation in the pixel DCR, PDP and fill factor. However, since all pixels in the imager are identical by design, it can be assumed that the fill factor of every pixel is the same. Hence, in this section DCR and PDP uniformity across the array are studied.

Dark count rate uniformity: For a SPAD-based photon detector, the main contributors to the DCR are the trap-assisted thermal noise and the band-to-band tunneling noise. The dependence of trap-assisted thermal noise on temperature and band-to-band tunneling noise on excess bias voltage has been studied and analyzed in detail for a SPAD array comprising 1024 SPADs in [7] [8] [9]. In this work, the variation in DCR across an array of 10,240 pixels is analyzed with respect to temperature and excess bias voltage. In this analysis the voltage across the SPAD (V_{op}) is used instead of the excess bias voltage to give a fair comparison between the observed DCR at various temperatures, as the SPAD breakdown voltage can also vary with temperature. The DCR uniformity in these experiments is evaluated by plotting the histogram of the DCR statistical distribution across the array. The experimental results of the DCR distribution at various temperature and excess bias voltages are shown in Figure 1.

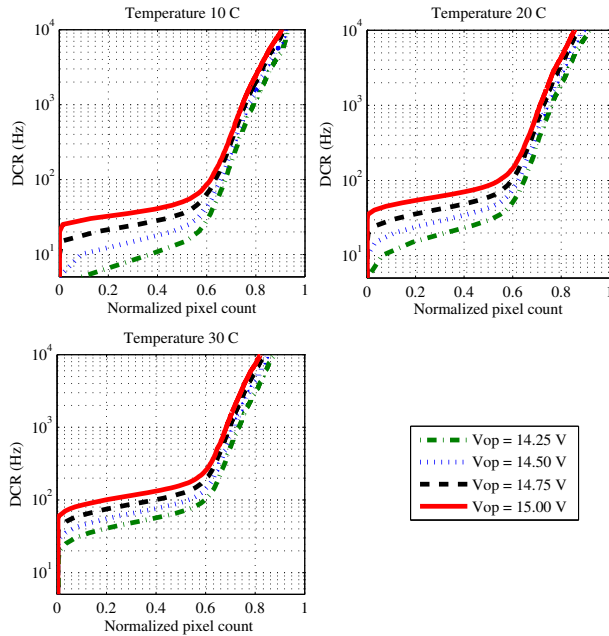


Fig. 1. DCR distributions

Figure 1 shows that with a SPAD bias voltage of 14.50 V at 20°C around 65% of the pixels have a DCR better than 200 Hz. Since the imager is designed for photon-starved applications, only low-noise pixels are to be considered; hence, in this work, the pixels with a DCR greater than 200 Hz are ignored. The noisy pixels correspond to around 35% of the total pixel count. The one sigma variation in DCR is about 40 Hz for the SPADs with a DCR less than 200 Hz. As Figure 1 shows, the median DCR of the pixel array decreases

with decreasing V_{op} and also with decreasing temperature, matching previous results [7] [8] [9]. The median DCR of the array can be reduced to around 20 Hz at 10°C with a V_{op} of approximately 14.25 V. A DCR decrease of this magnitude implies that the noise is predominantly trap-assisted thermal noise.

PDP uniformity: The photon detection probability, which is the probability that a photon incident on the SPAD's active area causes an avalanche, depends on the wavelength of the incident light, the temperature, and the applied voltage. The uniformity in PDP at a given wavelength of the incident light can be analyzed by studying the variation in the excess bias voltage available across the SPAD array. It can vary only if there is a variation in the breakdown voltage V_{bd} across the array, or if there is a variation in the applied SPAD bias voltage. The variation in V_{bd} across the array is shown in Figure 2.

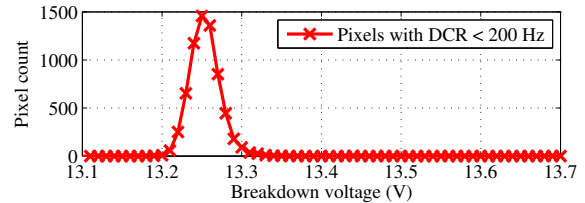


Fig. 2. SPAD V_{bd} distribution

Figure 2 shows a one sigma variation in V_{bd} under 50 mV. A 50 mV variation in V_{bd} will lead to a negligible variation in the PDP when the imager is operated with at least 1 V of excess bias. No obvious spatial pattern exists in the breakdown voltage variation. This observation implies that the routing or other fabrication specific systematic errors does not cause the 50 mV variation in V_{bd} .

Electrical noise's impact: To understand the effect of electrical noise on the DCR, the DCR across the active pixels is observed while varying the number of active columns. Deactivation of a column results not only in the deactivation of the corresponding I/O pad, but also the SPAD and the pixel circuitry on that column. As Figure 3 shows, there is negligible variation in DCR with respect to the number of active columns, implying that the DCR is exclusively due to intrinsic SPAD DCR mechanisms (trap assisted and tunneling), and is completely decoupled from the electrical noise (supply or substrate induced).

To investigate the impact of the digital noise in TUPC mode, a variation in the circuitry activity is induced by varying both the number of active columns and the light intensity. To compare the variations induced in the count rate at various intensities of light, the percentage increase in count rate was examined with respect to one column active. Figure 4 shows the variation in photon count observed in column one of the imager as a function of light intensity. In this analysis the light intensity is represented as median photon count rate observed across the pixels when one column was active. Usage of median count rate instead of light intensity helps generalize the

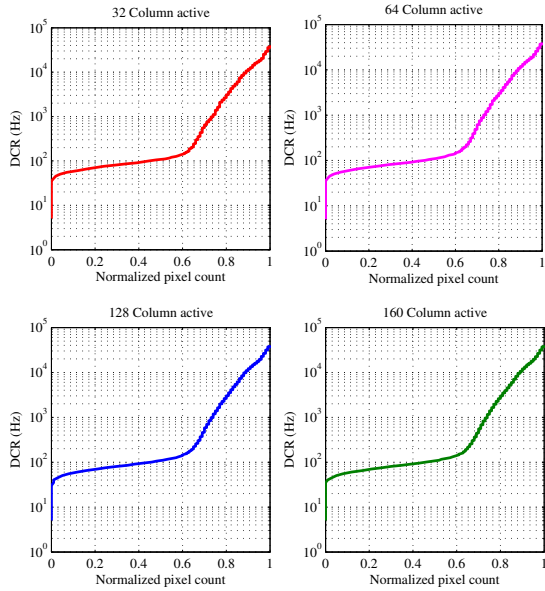


Fig. 3. Impact of electrical noise on DCR

results, and can be used to compare the performance of various SPAD-based imagers with varying fill factors and PDPs in the future.

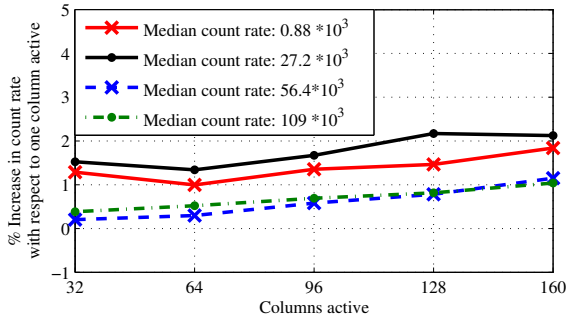


Fig. 4. Impact of digital noise on TUPC mode

Figure 4 shows that the percentage variation in the count rate is negligible with an increasing number of active columns, implying that the effect on digital noise on the TUPC mode of operation is negligible.

III. TIME-CORRELATED SINGLE-PHOTON COUNTING MODE

In time-correlated single-photon counting (TCSPC) mode, a TDC measures the photon arrival time relative to an external reference signal. In this section, TDC timing measurement uniformity across the array is presented.

Variation in TDC resolution: Figure 5 presents the observed variation in the TDC resolution across 160x64 pixels. From the plot it can be interpreted that the median TDC resolution is 55ps and one-sigma variation is about 2 ps. The observed variation in TDC resolution could be due to the

process variation. However the observed variation in the TDC resolution can be corrected by post-processing the TDC output.

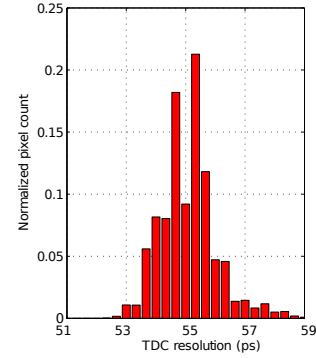


Fig. 5. Variation in TDC resolution

Timing jitter variation: The 20,480 TDCs present on-chip are designed to operate in parallel. However, even with the reverse START-STOP technique used in the imager [10], it is unlikely to reach a scenario in a photon-starved application when all the TDCs are active at the same time. To investigate the impact on the photon time-of-arrival measurement with a varying number of active TDCs, a study is carried out with varying light intensity and active pixel count. For this investigation a pulsed laser source operating in a mode synchronous with the TDC stop signal is used, and the statistical variation in the TDC output is then evaluated.

The impact of supply/substrate noise on timing performance is assessed by analyzing the pixel timing jitter. In this analysis the variation in circuit activity is induced by varying active pixel counts and light intensity. Figure 6 presents the experimental evaluation of timing jitter with varying circuit activity. The plot on the left presents the timing performance of a pixel under a light intensity corresponding to 19kHz median photon count rate with varying number of active columns.

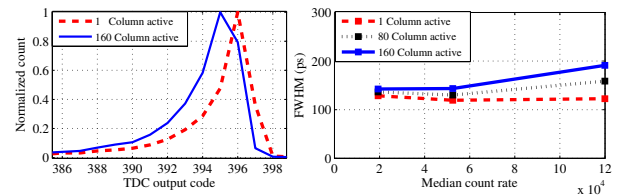


Fig. 6. Pixel timing performance variation without PVT compensation

Figure 6 on the right, implies that the worst case jitter variation corresponds to 70ps. A variation of 70ps in timing jitter was observed under a light intensity corresponding to a median photon count rate of 120 kHz, which is very unlikely to be observed in a photon-starved application. The variation in jitter and optical spike location with varying light intensity and active pixels can be due to the supply/substrate noise. To reduce the impact of the supply/substrate noise on the timing performance, the imager was evaluated by enabling the process, voltage, and temperature (PVT) feedback control loop, which is located on-chip. Figure 7 represents the pixel

timing performance with PVT compensation on. Figure 7 shows the variation in the timing jitter with varying pixel count and light intensity. The plot on the left represents timing performance of one pixel with varying number of active columns under a light intensity corresponding to 14kHz. It should be noted that with PVT enabled, the median TDC resolution changes to 87ps from 55ps. Although, the median TDC resolution does indeed increase with PVT enabled, there is basically negligible overall jitter variation (Figure 7 right).

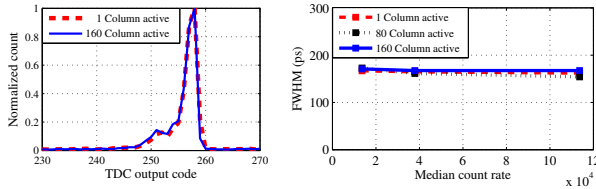


Fig. 7. Pixel timing performance variation with PVT compensation enabled

Timing jitter distribution: Figure 8 and Figure 9 show the temporal position of the optical spike and its jitter distribution across the array. These results were obtained by activating all the pixels with the median photon count rate of approximately 36 kHz. It should be noted that this experiment was carried out using a red laser (637 nm), with PVT enabled. Figure 8 shows a gradual variation in the temporal position of the optical spike toward the center of the array. This variation is caused by the propagation delay of the TDC STOP signal entering the array from either ends of the imager.

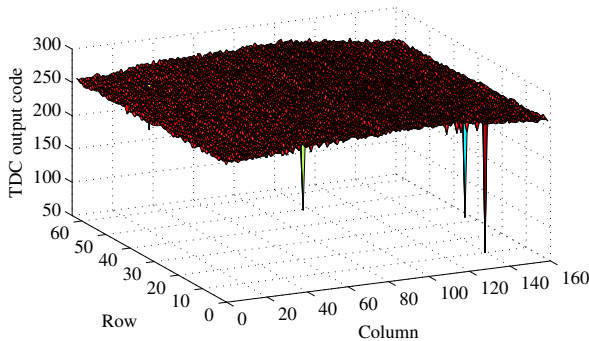


Fig. 8. Distribution of optical spike centroid variation in terms of TDC output code, with a TDC resolution of 87ps

Figure 9 shows a one-sigma variation in pixel-jitter of about 40 ps for low DCR pixels. In case of noisy pixels, the noise floor introduced by the DCR and the background noise increased to a level such that FWHM cannot be determined. From the experimental results it was found that the median jitter across the array was 180 ps with PVT, and 140 ps without enabling PVT.

IV. CONCLUSION

A 160x128 SPAD-TDC array has been characterized for photon detection uniformity and timing uniformity across the array in a photon-starved regime, suited for applications such

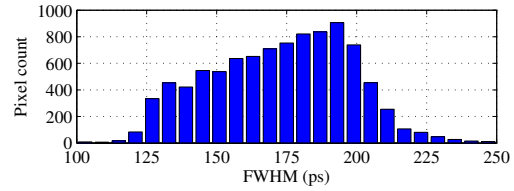


Fig. 9. Distribution of pixel timing jitter with PVT compensation enabled

as FLIM, FCS, and FRET. The characterization results have shown a negligible error of 2.5% in photon detection with increase in active pixel count. Furthermore, the median TDC resolution across the array is found to be 55ps with a standard deviation under 2 ps. Under photon-starved conditions, the median pixel timing jitter is 140ps. A negligible variation in photon detection uniformity and timing performance across the array has shown that the imager is well suited for photon-starved applications.

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REFERENCES

- [1] S. Cova et al., *Towards picosecond resolution with single-photon avalanche diodes*, Review of Scientific Instruments, 52 (3), pp. 408-412, 1981
- [2] C. Niclass et al., *Design and Characterization of a CMOS 3-D Image Sensor based on Single Photon Avalanche Diodes*, IEEE Journal of Solid-State Circuits, Vol. 40, N. 9, pp. 1847-1854, Sep. 2005.
- [3] D. Stoppa et al., *A CMOS 3-D Imager based on Single Photon Avalanche Diode*, IEEE Trans. On Circuits and Systems I, Vol. 54, N. 1, pp. 4-12, Jan. 2007.
- [4] S. Tisa et al., *100kframe/s 8 bit Monolithic Single-Photon Imagers*, IEEE European Solid-State Device Conference (ESSDERC), pp. 274-277, Sep. 2008.
- [5] B. Aull, et al., *Laser Radar Imager based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers*, IEEE ISSCC, pp. 238-239, Feb. 2006.
- [6] C. Niclass et al., *A 128x128 Single-Photon Image Sensor with Column-Level 10-bit Time-to-Digital Converter Array*, IEEE Journal of Solid-State Circuits, Vol. 43, N. 12, pp. 2977-2989, Dec. 2008.
- [7] J. Richardson et al., *A 32x32 50ps Resolution 10 bit Time to Digital Converter Array in 130nm CMOS for time Correlated Imaging*, IEEE Custom Integrated Circuits Conference, Sep. 2009.
- [8] M. Gersbach et al., *A Parallel 32x32 Time-to-Digital Converter Array Fabricated in a 130nm Imaging CMOS Technology*, IEEE ESSCIRC, Sep. 2009.
- [9] D. Stoppa et al., *A 32x32-Pixel Array with In-Pixel Photon Counting and Arrival Time Measurement in the Analog Domain*, IEEE ESSCIRC, Sep. 2009.
- [10] C. Veerappan et al., *A 160x128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter*, ISSCC, Feb. 2011.
- [11] D.U. Li et al., *Real-time fluorescence lifetime imaging system with a 32 32 0.13m CMOS low dark-count single-photon avalanche diode array*, Optics Express, Vol. 18, 2010.