

# RTS Noise Characterization in Single-Photon Avalanche Diodes

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**Abstract**—Random telegraph signal (RTS) behavior is reported and characterized in the dark count rate of single-photon avalanche diodes (SPADs). The RTS is observed in a SPAD fabricated in 0.8- $\mu\text{m}$  CMOS technology and in four proton-irradiated SPADs designed and fabricated in 0.35- $\mu\text{m}$  CMOS technology. The RTS characteristics are evaluated experimentally and verified theoretically with respect to bias and temperature.

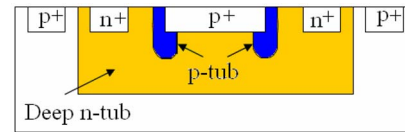
**Index Terms**—Dark count rate (DCR), random telegraph signal (RTS), single-photon avalanche diodes (SPADs).

## I. INTRODUCTION

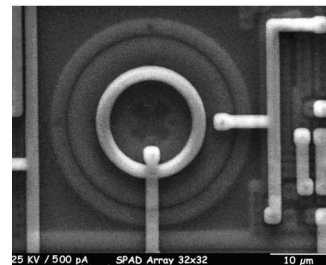
WHEN the charge transport through a solid-state device is controlled by changing the state of a trap, defect, or cluster of defects, it gives rise to a discrete switching of the current, called burst or popcorn noise, or, more often, random telegraph signal (RTS) [1]. Although RTS is important for small-area scaled devices, researchers have shown that the superposition of RTSs will result in flicker ( $1/f$ ) noise in large devices [2].

Among solid-state single-photon detectors, CMOS single-photon avalanche diodes (SPADs) are effective in a number of applications, including rangefinding, fluorescence detection, and high-speed imaging [3]. A SPAD is generally implemented as a p-n junction biased above breakdown so as to operate in the so-called Geiger mode. Fig. 1 shows the cross section of a particular implementation of a SPAD in some planar processes. In the Geiger mode of operation, photo-generated carriers may cause an avalanche by impact ionization, and correspondingly, a current pulse of appreciable amplitude is generated. Tunneling, Shockley–Read–Hall (SRH) generation, and afterpulsing are the three main noise sources in SPADs; these sources can be isolated by observing the statistical properties and temperature dependence of the devices [4]. The noise performance of SPADs is mainly characterized by dark counts, which are spurious pulses quantified in terms of mean frequency or dark count rate (DCR) [5].

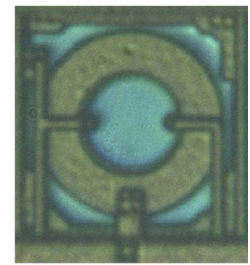
Understanding and modeling DCR instability may provide a powerful tool to predict and analyze defects in standard



(a)



(b)



(c)

Fig. 1. (a) SPAD cross section. (b) SEM image of a SPAD implemented in 0.8- $\mu\text{m}$  CMOS process. (c) Photomicrograph of a SPAD implemented 0.35- $\mu\text{m}$  CMOS process.

CMOS processes while suggesting new techniques to overcome their effects by design. In this letter, we describe temporal fluctuations of DCR between different states in SPADs. The statistics of such a fluctuation follows an RTS behavior.

## II. RANDOM TELEGRAPH NOISE

RTS phenomena have been observed in currents of MOSFETs, JFETs, DRAMS, proton-irradiated CCDs, neutron-irradiated avalanche photodiodes, and proton- and heavy-ion-irradiated active pixel sensors [6], [7]. Moreover, the presence of individual bistable defects in APDs and neutron-irradiated APDs was suggested when the APDs were biased 10 V above their 250-V breakdown voltage [8].

The different configuration of a trap, defect, or cluster of defects causes the superposition of several levels of fluctuation (multistable) or a two-level fluctuation [9]. The bias and temperature dependence of a bistable RTS was analyzed in a SPAD design fabricated in 0.8- $\mu\text{m}$  CMOS technology [10].

Fig. 2 shows DCRs for three different proton-irradiated pixels of a SPAD fabricated in the 0.35- $\mu\text{m}$  CMOS technology. While the third pixel shows a standard bistable behavior, the other two show multistable and multibistable behaviors. The autocorrelation and temperature behavior of DCR fluctuations enabled us to show that RTS is free from afterpulsing [10]. Moreover, the power spectral density of DCR shows a Lorentzian spectrum, which is a necessary but not sufficient condition of RTS signals [10]. In addition, the power spectral density of DCR in some pixels shows different configurations of traps or defects, causing the multistable behavior, as shown in Fig. 3 [11].

A simple two-level RTS is defined by three parameters: the time spent in the up (or high) state ( $t_u$ ), the time spent in the down (or low) state ( $t_d$ ), and the amplitude [1].

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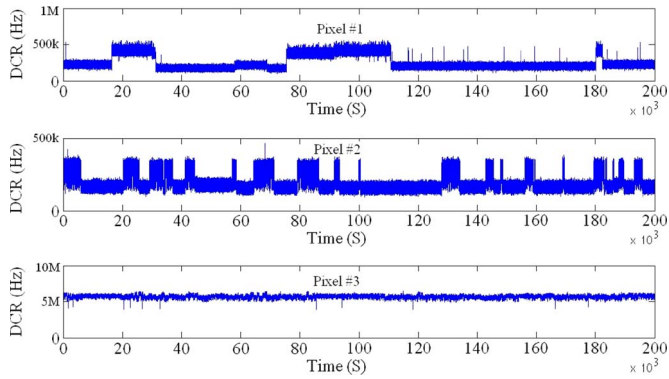


Fig. 2. Different forms of RTS in three pixels of a proton-irradiated SPAD.

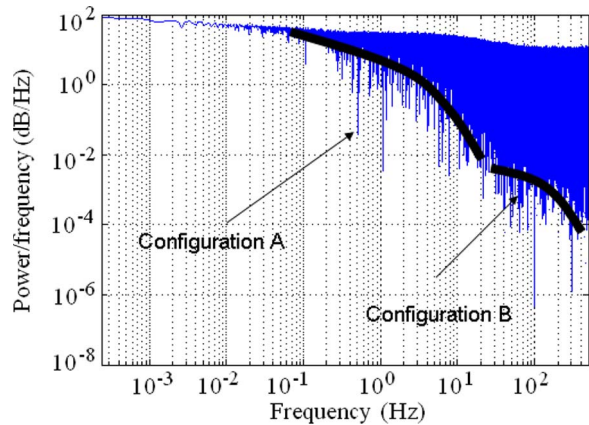


Fig. 3. Different configurations of traps or defects in the power spectral density of DCR.

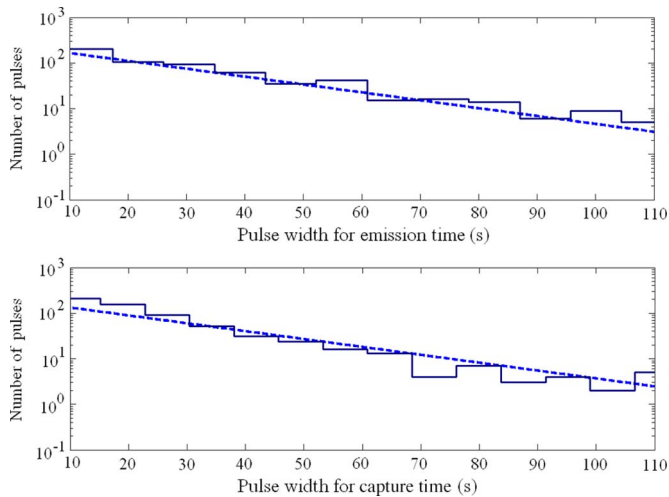


Fig. 4. Pulsewidth histograms obtained by sorting and counting the capture and emission times of a bistable pixel at room temperature for 8 h. The dashed lines are the expected number of pulses considering (1).

The exponential behavior in the time distributions of both up (capture) and down (emission) states is in accordance with (1) [1]. In this equation,  $P_{\text{up,down}}$  is the probability of up or down state in a typical RTS. Fig. 4 shows the matching of the pulsewidth histogram of the RTS behavior with the exponential characteristic considering the emission time of 25 s and the capture time of 18 s

$$P_{\text{up,down}}(t) = \frac{1}{\tau_{\text{up,down}}} \exp\left(-\frac{t}{\tau_{\text{up,down}}}\right). \quad (1)$$

TABLE I  
ACTIVATION ENERGY OF THE PIXELS CONTAINING TRAPS AND DEFECTS

$E_{\text{act}}$ (eV)	Up state	Down state
0.8 $\mu\text{m}$ chip	0.6108	0.7233
Pixel #1	0.4592	0.4286
Pixel #3	0.5243	0.4572

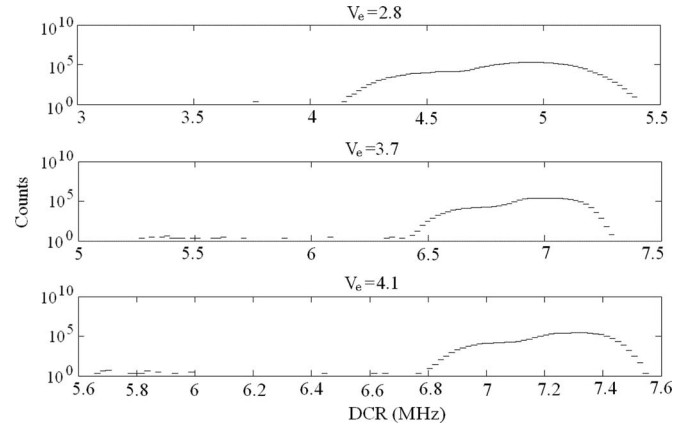


Fig. 5. DCR histogram of pixel #3 showing the number of DCR levels increasing as a function of excess bias voltage.

### III. RESULTS AND DISCUSSION

The RTS behavior was observed in a pixel of a  $32 \times 32$  SPAD imager designed and implemented in  $0.8\text{-}\mu\text{m}$  CMOS technology and in four pixels of a  $32 \times 32$  SPAD imager designed and implemented in  $0.35\text{-}\mu\text{m}$  CMOS technology. The latter was irradiated with an 11-MeV proton source [3], [12]. The activation energy for traps and defects are shown in Table I. The activation energies are calculated by considering the Arrhenius equation [9]

$$\frac{1}{\tau_{\text{up,down}}} = R e^{-E_{\text{act}}/kT}. \quad (2)$$

In this equation,  $E_{\text{act}}$  is the activation energy,  $R$  is the rate constant, and  $\tau$  is the time constant for the up and down states.

Analyzing the RTS behavior of the pixels by increasing the reverse-bias voltage shows the appearance of new DCR levels in the DCR histogram (Fig. 5).

By considering the low probability of multiple electron trapping at one defect site in conventional sensors [13], the appearance of these new levels is due to the existence of a second trap with a slightly different energy level. This trap causes the emergence of a new DCR level when the excess bias voltage reaches a certain threshold. Moreover, the shift in the frequency of the DCR in the figure with regard to excess bias voltage is due to the increase in breakdown probability. It should be noted that the independence of jump time is due to the distinct lifetime of each configuration of traps, defects, or cluster of defects.

In addition, the number of distinct DCR levels in the histogram is temperature dependent, which can be due to the different locations of traps in the band diagram, as shown in Fig. 6. In places where the SRH center is above the quasi-Fermi level, increasing the temperature will increase the probability of filling the SRH center, thus decreasing the number of distinct DCR levels. In contrast, when the location of the SRH center is below the quasi-Fermi level, an increase of temperature

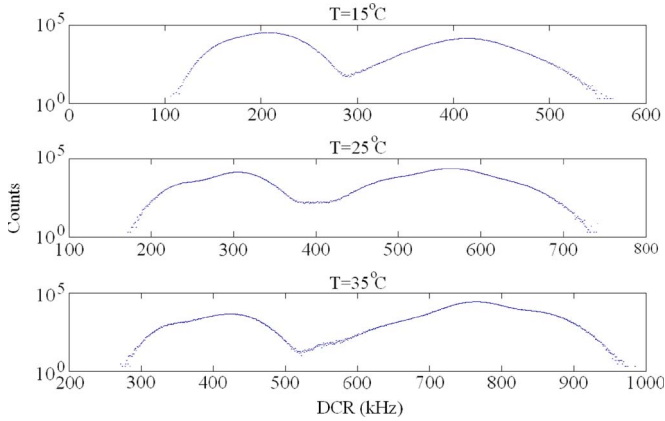


Fig. 6. DCR histogram of pixel #1 showing the number of DCR levels increasing as a function of temperature.

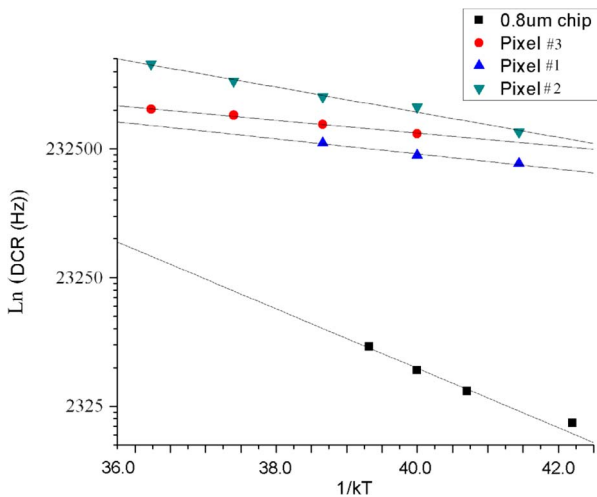


Fig. 7. DCR RTS amplitude versus temperature in four different pixels at constant excess bias voltage. The fitting function is  $y = ae^{bx}$ , where  $a$  and  $b$  are equal to  $3.3 \times 10^{12}$  and  $-0.53$  for an  $0.8\text{-}\mu\text{m}$  chip,  $3.75 \times 10^5$  and  $-0.022$  for pixel #3,  $2.04 \times 10^7$  and  $-0.1352$  for pixel #1, and  $1.92 \times 10^6$  and  $-0.05$  for pixel #2, respectively.

decreases the probability of filling the trap and correspondingly increases the number of distinct DCR levels. Another reason for the creation of new DCR levels with the increase of temperature could be the expansion of the depletion region.

Fig. 7 shows the temperature dependence of the RTS amplitude. The 1-D Poole–Frenkel theory describes RTS variation in the electrical current of devices by introducing a factor  $\chi$ , which is exponentially dependent on temperature [14]. We have observed the same behavior but in DCR, which can be explained by the same theory.

Fig. 8 shows the increase in RTS amplitude as a function of excess bias voltage. In conventional trap-assisted tunneling model, the increase of electric field is being described by considering the time constants for tunneling between the valence or conduction band ( $\tau_t$ ) and the trap [15]. This variation in tunneling time constant describes the increase in electrical current of the device. We have observed the same behavior in DCR, which can be explained by the same theory.

#### IV. CONCLUSION

This letter has reported on DCR bistability and multistability in CMOS SPADs and proton-irradiated SPADs. Statistical

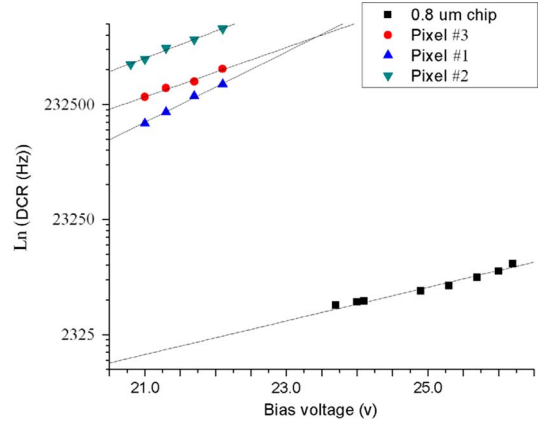


Fig. 8. DCR RTS amplitude versus bias voltage at room temperature. The fitting function is  $y = ae^{bx}$ , where  $a$  and  $b$  are equal to 0.5783 and 0.336 for an  $0.8\text{-}\mu\text{m}$  chip, 3.52 and 0.4954 for pixel #3, 0.026 and 0.704 for pixel #1, and 2.89 and 0.541 for pixel #2, respectively.

analysis of the phenomenon reveals that it follows an RTS behavior. The RTS hypothesis was verified by measurements that are in excellent agreement with the theory.

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