A first single-photon avalanche diode fabricated in standard SOI CMOS technology with a full characterization of the device

Myung-Jae Lee,[*] **Pengfei Sun, and Edoardo Charbon**

Faculty of Electrical Engineering, Delft University of Technology, Mekelweg 4, 2628 CD Delft, the Netherlands
[*]*M.J.Lee@tudelft.nl*

Abstract: This paper reports on the first implementation of a single-photon avalanche diode (SPAD) in standard silicon on insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology. The SPAD is realized in a circular shape, and it is based on a P^+/N-well junction along with a P-well guard-ring structure formed by lateral diffusion of two closely spaced N-well regions. The SPAD electric-field profile is analyzed by means of simulation to predict the breakdown voltage and the effectiveness of premature edge breakdown. Measurements confirm these predictions and also provide a complete characterization of the device, including current-voltage characteristics, dark count rate (DCR), photon detection probability (PDP), afterpulsing probability, and photon timing jitter. The SOI CMOS SPAD has a PDP above 25% at 490-nm wavelength and, thanks to built-in optical sensitivity enhancement mechanisms, it is as high as 7.7% at 850-nm wavelength. The DCR is 244 Hz/μm^2, and the afterpulsing probability is less than 0.1% for a dead time longer than 200 ns. The SPAD exhibits a timing response without exponential tail and provides a remarkable timing jitter of 65 ps (FWHM). The new device is well suited to operate in backside illumination within complex three-dimensional (3D) integrated circuits, thus contributing to a great improvement of fill factor and jitter uniformity in large arrays.

OCIS codes: (040.1345) Avalanche photodiodes (APDs); (040.0040) Detectors; (130.3120) Integrated optics devices; (040.3780) Low light level; (280.4788) Optical sensing and sensors; (040.5160) Photodetectors; (230.5170) Photodiodes; (040.5250) Photomultipliers; (030.5260) Photon counting; (130.5990) Semiconductors; (130.6010) Sensors; (040.6040) Silicon; (050.6875) Three-dimensional fabrication.

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1. Introduction

Recently, silicon single-photon avalanche diodes (SPADs) based on standard complementary metal-oxide-semiconductor (CMOS) technology have received a great amount of attention by scientific and also industrial communities, because their compatibility with standard processes makes SPADs a cost-effectiveness solution to applications requiring photon-counting and photon-starved imaging. Examples of such applications include positron emission tomography (PET), single-photon emission computed tomography (SPECT), fluorescence-lifetime imaging microscopy (FLIM), fluorescence correlation spectroscopy (FCS), time-of-flight (TOF) three-dimensional (3D) imaging, etc. [1–5]. Due to the dynamic nature of single-photon detection, in situ processing is often a preferred solution, but the monolithic integration of SPADs and electronic circuits results in relatively low fill factor, which is the ratio of photon-sensitive area to total area in an image sensor.

In order to increase fill factor, there has been growing interest in backside-illumination (BSI) SPADs, possibly involving 3D integration schemes [5, 6]. BSI solutions may greatly increase fill factor and pixel density and consequently enable much better photon statistics and higher quality imaging. In general, however, CMOS-compatible SPADs have been implemented using a bulk silicon wafer, which makes it difficult to realize the BSI SPADs for the 3D-integration scheme without modifying the fabrication process. On the other hand, implementation of SPADs using standard silicon on insulator (SOI) CMOS technology can be an attractive solution, because the buried oxide (BOX) layer in the SOI wafer can be easily used as an etching stop during the wafer backside etching process. However, to the best of our knowledge, no SPAD has yet to be demonstrated in a standard deep-submicron SOI CMOS

technology. Recently, Zou *et al.* has reported a SPAD fabricated in 0.35-μm SOI CMOS technology for a wafer-to-wafer bonding 3D structure, but only dark count rate (DCR) and current-voltage characteristics of the SPAD were reported without any further characterization [6].

In this paper, we present the first SPAD fabricated in standard deep-submicron SOI CMOS technology complete of a full characterization of the device. The fabricated SPAD has a photon detection probability (PDP) of 25.4% at 490-nm wavelength with PDP enhancement at around 800-nm wavelength. The DCR is 244 Hz/μm^2, afterpulsing probability is less than 0.1% with a 200-ns dead time, and timing jitter is a record 65 ps at room temperature and 3-V excess bias voltage.

2. Device structure and simulation

Figure 1 shows a cross section of the SPAD. It was fabricated in standard 140-nm SOI CMOS technology, in which thicknesses of the BOX layer and silicon layer over the BOX are about 1 μm and 1.5 μm, respectively. N-well and P-well are deposited over the p-type epi layer, because it is not based on substrate.
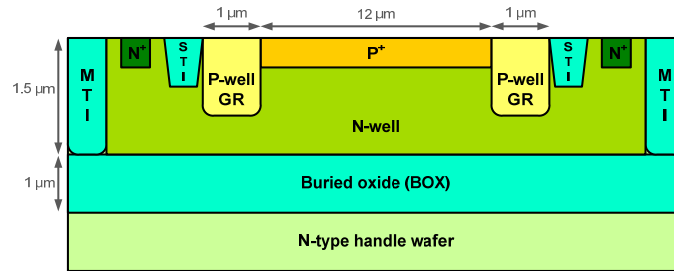

Fig. 1. Cross section of the fabricated SOI CMOS SPAD (MTI: medium trench isolation, STI: shallow trench isolation).

The SPAD was realized in a circular shape based on a P^+/N-well junction with an active-area diameter of 12 μm. Shallow trench isolation (STI), generally provided in CMOS process technology nodes of 250 nm and smaller, can be used as a guard-ring (GR) structure to achieve the largest electric field at the junction [7], but in general it can bring high DCR due to etching-induced lattice defects and charge trapping associated with STI [8]. In the proposed SPAD, a merged implant GR structure was used to prevent premature edge breakdown, implemented by lateral diffusion of two closely spaced N-well regions. The width of the P-well GR was designed to have a 1 μm width, considering the lateral diffusion length of the N-well. Most importantly, *no process modification was required*, so as to make the device fully compatible with the requirements of reliability of industrial SOI CMOS processes.

In order to investigate the effect of the GR structure and the electric field profiles at the planar junction, we performed device simulation with MEDICI, as shown in Fig. 2. It shows the simulated electric-field distribution when the SOI CMOS SPAD is biased above its breakdown voltage for Geiger-mode operation. As can be seen in this figure, the premature edge breakdown is effectively suppressed by the P-well (PW) GR. Consequently, the electric field is high enough (over 6×10^5 V/cm) to ensure impact ionization all over the planar junction, which is much higher than the breakdown field in silicon of 3×10^5 V/cm [9].
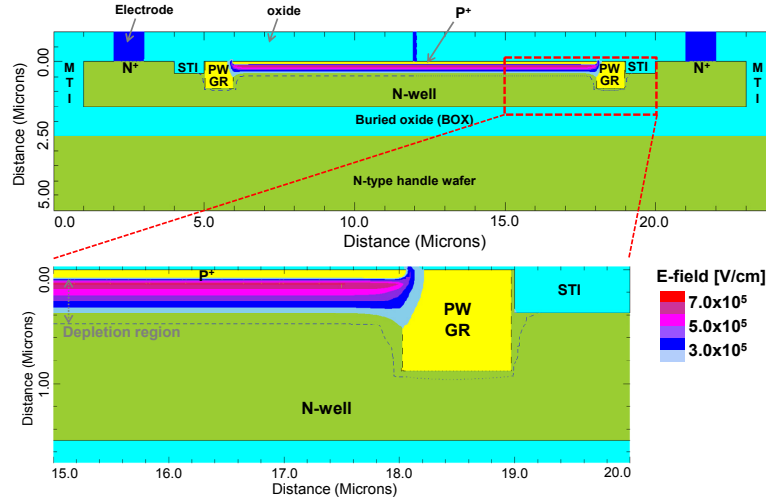
Fig. 2. Electric field in a SPAD biased above breakdown by an excess bias voltage V_E of 3 V.

3. Experimental results

For the SOI CMOS SPAD characterization, the SPAD chip was packaged and then measured. Because the SPAD is connected to PADs directly, it was operated in Geiger mode using a passive quenching resistor of about 20 kΩ. The P$^+$/N-well junction is reverse biased with a positive voltage applied to the N-well contact, which is the sum of its breakdown voltage, V_B, and an excess bias voltage, V_E, and the P$^+$ contact is connected to the quenching resistor. Then the P$^+$ contact is connected to a high-performance oscilloscope to measure DCR, PDP, afterpulsing probability, and photon timing jitter. Measurements were done at room temperature except when indicated otherwise.

3.1. I-V characteristics

The I-V characteristic of the fabricated SPAD was firstly measured to check its breakdown voltage and consequently to measure the SPAD at the correct excess bias conditions. As shown in Fig. 3, the SPAD exhibits very low dark current, below 1 pA, before avalanche breakdown at about 11.3 V, where the current starts to increase drastically due to the avalanche multiplication process. The SPAD's breakdown voltage indicates a relatively high doping concentration of N-well at around 10^{17} cm^{-3} in this technology. In addition, it is experimentally demonstrated that the SPAD could not operate above about 23 V because the depletion region below the P-well GR reaches the BOX layer.
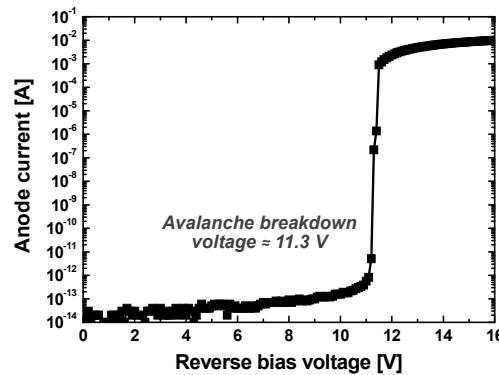

Fig. 3. Steady-state current-voltage characteristics under dark conditions at room temperature.

3.2. DCR

Figure 4 shows DCR characteristics of the SPAD measured at the different excess bias voltages in the dark; the DCR varies from a minimum of 1.1 Hz/μm^2 to a maximum of 244 Hz/μm^2, at room temperature. Figure 4(b) shows the Arrhenius plot of DCR at three different excess bias voltages. DCR exhibits weak dependence on temperature, which indicates that the contribution of band-to-band tunneling to the DCR is much higher than that of Shockley-Read-Hall (SRH) thermal generation [2]. In addition, the low activation energies, $E_a = 0.129$, 0.105, and 0.082 eV, for the three excess bias voltages estimated from Fig. 4(b) are accordance with the band-to-band tunneling. We believe that a relatively high doping concentration of the N-well is responsible for this behavior, as confirmed by the I-V characteristics of Fig. 3. The DCR of this device is comparable to or about one order of magnitude higher than that of SPADs fabricated in bulk wafers. However, the DCR is similar to or better than that of SPADs based on SOI wafers in non-standard processes which is in the range between 3.5 kHz and 100 kHz [6, 10, 11].
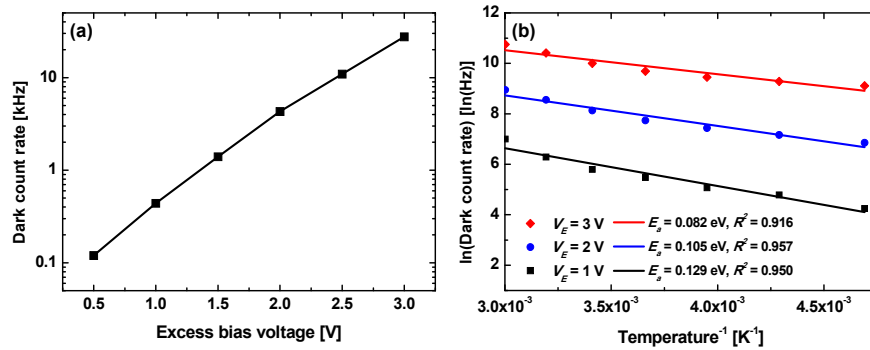

Fig. 4. DCR (a) as a function of the excess bias voltage at room temperature and (b) as a function of the inverse of temperature for various excess bias voltages.

3.3. PDP

The measured PDP for incident-light wavelengths from 400 nm to 950 nm at three different excess bias voltages are plotted in Fig. 5. The SOI CMOS SPAD has a maximum PDP of about 25.4% at the 490-nm wavelength. Then, the PDP decreases for longer wavelengths because of the longer penetration depth of photons than the shallow P$^+$/N-well junction. However, it still provides 7.7-% PDP at the 850-nm wavelength where silicon has very low absorption coefficient, because the PDP of the SOI CMOS SPAD is enhanced at long wavelengths due to the cavity-like behavior of the interface between silicon and BOX layers. Such effect has been also reported in [10, 11].
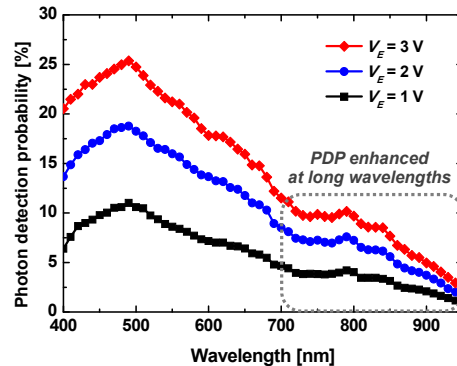

Fig. 5. PDP as a function of wavelength for various excess bias voltages at room temperature.

3.4. Afterpulsing probability

Afterpulsing is caused by carriers that were trapped in previous avalanches and that trigger spurious avalanches. The afterpulsing statistics of the SOI CMOS SPAD was measured using an inter-arrival time histogram method [12]. Figure 6 shows the measured inter-arrival time histogram of the SPAD with a fitted exponential curve. The afterpulsing probability is computed as the area between the histogram and the fitted exponential curve; in this device this value is about 1.7% setting a 100-ns dead time, but it can be further reduced down to 1% by increasing the dead time to 200 ns.
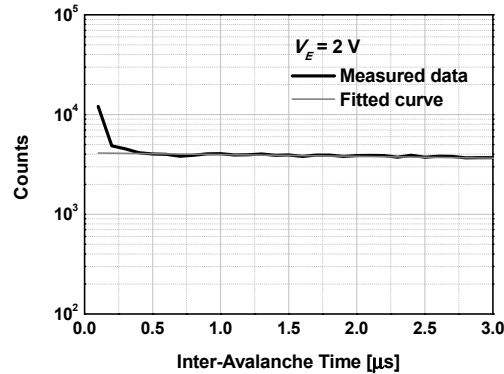

Fig. 6. Afterpulsing: inter-arrival time histogram measured at room temperature and exponential curve fit.

3.5. Timing jitter

Timing jitter is defined as the uncertainty of time response of the SPAD to photons impinging the device. The time response was measured using the time-correlated single-photon counting (TCSPC) technique, whereas a fast laser source (Advanced Laser Diode Systems GmbH) at 405 nm and a repetition rate of 40 MHz was used. The histogram of the time interval between the laser output trigger and the SPAD raising edge was measured using an oscilloscope (LeCroy WavePro 760Zi-A) operating as a time-to-digital converter with a time bin of 2 ps (LSB). The resulting normalized histograms are shown in Fig. 7 for several excess bias voltages. The single-photon time resolution (SPTR) is as low as 65 ps (FWHM) for $V_E = 3$ V, and it degrades, as expected, at lower excess bias voltages. The measured laser timing jitter was about 25 ps.
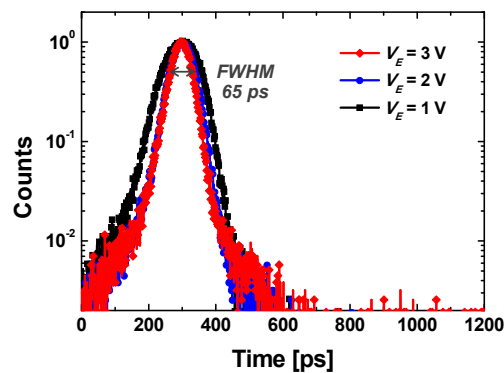

Fig. 7. Timing jitter performance as a function of excess bias voltage at room temperature using a 405-nm wavelength laser.

4. Comparison with the state-of-the-art CMOS SPADs

In general, deep-submicron SPADs have many advantages such as smaller pixel size, better timing resolution, larger array, higher speed, and higher fill factor. At the same time, however, there are also some disadvantages: lower and narrower PDP as well as higher tunneling noise due to higher doping concentrations. In order to compare performance of the proposed SPAD fabricated in 140-nm SOI CMOS technology to the literature in similar technology nodes, we restricted our attention to all reported substrate-isolated SPADs implemented in a feature size smaller than 250 nm [4, 13–18]. Consequently, SPADs fabricated in 350-nm CMOS technology are excluded in this comparison, although they exhibit good performance [19–21]. The reason for ruling out non-substrate-isolated SPADs is that they are not suitable for array configurations and for integration with electronic circuits in the same substrate due to high optical crosstalk and electrical interference from digital circuits [4, 22, 23].
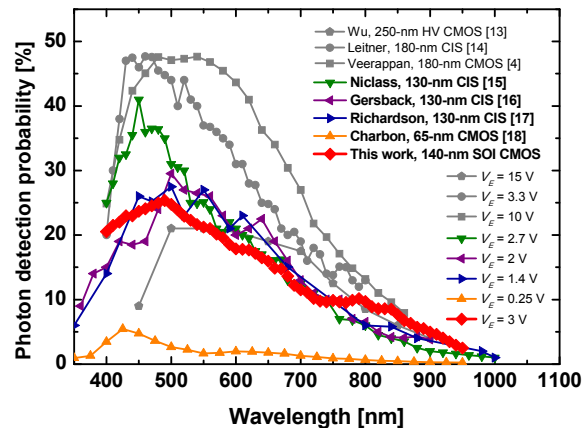

Fig. 8. SPAD-performance comparison: PDP.

Figure 8 shows a PDP-performance comparison. The SPAD reported by Veerappan *et al.* shows a high and wide PDP profile due to the wide depletion region using a deep N-well (DNW) having a lower doping concentration and very high excess bias voltage [4]. Leitner *et al.* and Niclass *et al.* also reported SPADs providing relatively high PDP because of a retrograde DNW and optimized dielectrics for optical detection, respectively, supported by the CMOS image sensor (CIS) technologies [14, 15]. Compared to other CMOS SPADs, the SOI CMOS SPAD exhibits medium PDP at short wavelengths but overperforms most SPADs in the literature above 750 nm.
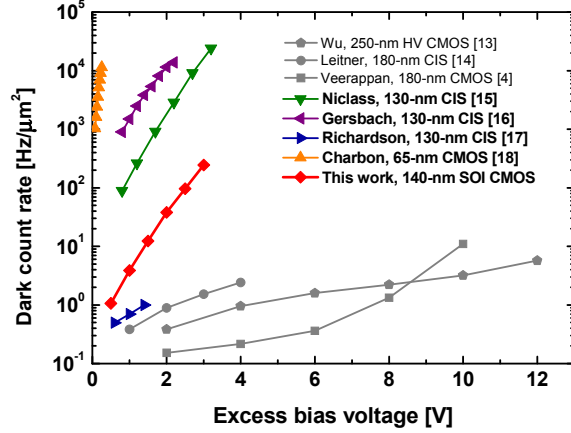
Fig. 9. SPAD-performance comparison: area-normalized DCR.

Figure 9 presents a DCR-performance comparison with the state-of-the-art CMOS SPADs. The SPADs fabricated in feature sizes larger than 180 nm tend to show better DCR performance. This is generally attributed to the fact that advanced CMOS technologies use narrower depletion widths and higher doping levels, which in turn cause higher band-to-band tunneling dark counts. Richardson *et al.* achieved low DCR using a low-doped P-well/retrograde DNW junction in the 130-nm CIS technology [17]. Compared with the similar-structure SPADs, which are based on P^+/N-well or N^+/P-well junctions, the DCR of the SOI CMOS SPAD is better than that of other SPADs implemented in 130-nm or 65-nm technologies. The state-of-the-art comparison of SPADs in terms of peak PDP and DCR is presented in Fig. 10.
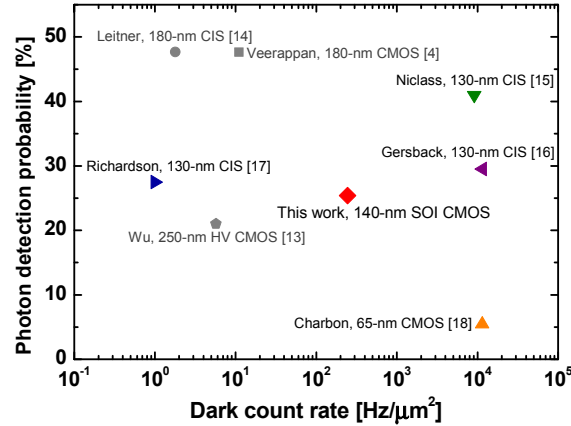

Fig. 10. SPAD-performance comparison: peak PDP vs. area-normalized DCR.

The performance of the SPAD implemented in the standard 140-nm SOI CMOS technology reported in this paper is summarized in Table 1. In addition, it reports a performance comparison with substrate-isolated SPADs fabricated in advanced CMOS technologies (140-nm technology nodes and below).

Table 1. Performance summary and comparison with substrate-isolated SPADs fabricated in advanced CMOS technologies (140-nm technology nodes and below)

	This work	[15]	[16]	[17]	[18]
Technology	140-nm SOI CMOS Technology	130-nm CMOS Imaging Process	130-nm CMOS Imaging Process	130-nm CMOS Imaging Process	65-nm CMOS Technology
PN junction GR structure	P$^+$/N-well P-well GR	P$^+$/N-well P-well GR	P$^+$/N-well P&STI GR	P-well/DNW virtual GR	N$^+$/P-well N-well GR
Active area (diameter)	113.1 μm^2 (12 μm)	87.5 μm^2 (10 μm)	58 μm^2 (8.6 μm)	50 μm^2 (8 μm)	56 μm^2 (8 μm)
Shape	Circular	Octagonal	Circular	Circular	Octagonal
V_B	11.3 V	9.7 V	9.4 V	14.4 V	9.1 V
V_E	3 V	2.7 V	2 V	1.4 V	0.25 V
DCR (@RT)	27.6 kHz 0.24 kHz/μm^2	800 kHz 9.1 kHz/μm^2	670 kHz 11.6 kHz/μm^2	50 Hz 1 Hz/μm^2	640 kHz 11.4 kHz/μm^2
PDP peak	25.4% (@490 nm)	41% (@450 nm)	30% (@500 nm)	28% (@500 nm)	5.5% (@425 nm)
PDP @850 nm	7.7%	3.8%	4.2%	5%	0.5%
Afterpulsing probability	< 0.1% (@200-ns dead time)	n.a.	< 1% (@180-ns dead time)	0.02% (@100-ns dead time)	< 1% (@5-μs dead time)
Timing jitter	65 ps (@405 nm)	144 ps (@637 nm)	125 ps (@637 nm) (@V_E = 1 V)	200 ps (@470, 815 nm)	235 ps (@637 nm) (@V_E = 0.4 V)

DNW: deep N-well, GR: guard ring, V_B: Avalanche breakdown voltage, V_E: Excess bias voltage, RT: room temperature

5. Conclusion

We presented the first SPAD fabricated in standard SOI CMOS technology. The SPAD has been simulated, fabricated, and fully characterized in relation to the literature. Despite relatively high doping concentrations and higher defectivity of the SOI wafer, the realized SPAD has a DCR of 1.1 Hz/μm^2 at 0.5 V and 244 Hz/μm^2 at 3 V of excess bias, which is comparable to or better than DCR of similar-structure SPADs, based on P$^+$/N-well or N$^+$/P-well junctions, fabricated in advanced bulk CMOS technologies. The SOI CMOS SPAD achieves a peak PDP over 25% at 490-nm wavelength, along with enhanced PDP performance at long wavelengths due to the interface between silicon and BOX layers that acts as an optical cavity. With a dead time longer than 200 ns, the SPAD exhibits a remarkably low afterpulsing probability of less than 0.1%, and moreover it shows an excellent SPTR of 65-ps FWHM. The SPADs based on standard SOI CMOS technology will enable to provide future 3D-integrated image-sensor solutions.

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