The Design of Micro-Electronic Circuits and Systems
Automation, physical verification

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TU Delft

From Walkman to iPod

[http://pocketcalculatorshow.com/walkman/sony]
Whole point is to put more and more functionality into a chip

Evolution

Intel 4004 (1971) and Itanium (McKinley, 2002) die compared to 2€ coin
Chip Anatomy

(Layout of chip, final design result)

(Rendering of) result after fabrication

Not 1-to-1, sorry

SEM Images

Cross-section

3d perspective
Design Challenge

- **System Complexity**
  Dealing with the sheer size of the system
  - > 10^6 components (transistors)
  - Compare boeing 747-400: 6x10^6 components
  - >> 10 km of interconnect
  - Compare boeing 747-400: 274 km wiring, 8 km tubing

- **Silicon Complexity**
  Dealing with the physical aspects
  - Features < 0.0000001 m = 100nm
  - Actually far from ideal behavior
    - More like building spaghetti bridges than steel bridges
  - Lots of unwanted parasitics
  - Manufacturing tolerances, …


How To Cope?

- **Abstraction and modeling**
  - Focus on separate issues of design at separate times
  - And by separate designers
  - What are proper abstractions?

- **Modularity and Reuse**
  - Decompose a design in manageable pieces
  - Make sure you can understand / handle pieces in part
  - … and their composition
  - … on all the relevant abstraction levels
  - Reuse modules whenever possible

- **Automation**
  - The computer is a designer’s best friend
  - Implement methodology and design flow
  - Electronic Design Automation is fantastic research field
Abstractions

<table>
<thead>
<tr>
<th>Behavior / Digital</th>
<th>Structure / Electrical</th>
<th>Physical / Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>NOT X</td>
<td>X</td>
<td>NOT X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

if x = '0' then
    reg1 <= a;
else
    reg1 <= b;
end if;

\[ i = C \frac{dV}{dt} \]
Generic Chip Design Flow

(1) if \( x = '0' \) then
(2) \( \text{reg1} \leftarrow a; \)
(3) else
(4) \( \text{reg1} \leftarrow b; \)
(5) end if;

Design Actions

Synthesis:
increasing information about the design by providing more
detail (within the same or another design domain).

Verification:
checking whether a synthesis step has left the specification
intact.

Analysis:
collecting information on the quality of the design.

Optimization:
increasing the quality of the design by rearrangements in a
given description.

Design Management:
storage of design data, cooperation between tools, design
flow, etc.
Electronic Design Automation is key enabling technology!
The software tools to do the actual IC design and engineering
These tools need to be designed and developed, too!
Need constant improvement to cope with technology progress
NVIDIA Example (A.D. 2000)

- ~850 employees (worldwide total incl. sales, mgmt, …)
- ~$85M of CAD tools
- ~$20M emulation
- Engineering Compute Resources
  - Desktops: 200 Sun / 2150 pc’s
  - Servers:
    278 Sun / 634 Linux / 496 Gbytes RAM
- 14 Terabytes of storage

1 Terabyte (TB) = 1000 GB
~ 1,000,000 large digital photos
~ 10 km of books on a shelf
~ 1 year of music ~ 200 iPods

NVIDIA - 2005

3000 compute servers

1700 engineers
2000 employees

440 TB Storage

84 TB data mirror in remote location

**Summarizing ...**

- System Complexity
- Silicon Complexity
- Abstraction and Modeling
- Modularity and Reuse
- Automation

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**My Research**

- **Main topic:** physical / electrical modeling of IC’s

- Design of IC’s is making approximations, assumptions, short-cuts, simplifications
- Real world physics is too complex to handle
- Need independent verification steps to check a design before fabrication
  - Will the chip actually work?
  - Is it within performance, power, reliability, etc. budget?

- See [www.space.tudelft.nl](http://www.space.tudelft.nl)

- You might remember this when choosing your MSc topic
**ASIC First Spin Errors**

- **Functional Logic Error**: 43%
- **Analog Tuning Issue**: 20%
- **Signal Integrity Issue**: 17%
- **Clock Scheme Error**: 14%
- **Reliability Issue**: 12%
- **Mixed Signal Problem**: 11%
- **Uses Too Much Power**: 11%
- **Has Path(s) Too Slow**: 10%
- **Has Path(s) Too Fast**: 10%
- **IR Drop Issues**: 7%
- **Firmware Error**: 4%
- **Other Problem**: 3%

**Source:**
Aart de Geus,
Chairman & CEO, Synopsis
ESNUG keynote, Sep 8, 2003

**Physical Verification**

**Layout-to-Circuit Extraction**

**Simulation**
Computation of Capacitance

Sysytematic, layout-process interaction based shape variability
- Has a pronounced effect on capacitance values
- Effect can be modeled with ‘local layout density’ concept
- (Effective) metal height

Unsolved Physical Verification Issue
Metal CMP Effects
Lithography Effects on C

From Ren et. al., CEM2006
- 90 nm technology, 193 nm litho
- About 5% difference in self-C
- About 9% difference for some coupling C
- Systematic effect, can be modeled in theory
- Need extraction solutions

My Lectures:
ET 4255 Electronic Design Automation

- Principles, methods, algorithms for Computer-Aided design of electronic systems
- Here: IC design
- Not about design
- But: how do I built the tools to do the design
- Lecture period: 4th quarter
Electronic Design Automation

- Principles, methods, algorithms for Computer-Aided design of electronic systems
- Here: IC design
- Not about design
- But: how do I built the tools to do the design

Why Education in EDA?

- Without EDA no chips
- Without chips no ...
- Without electrical engineers no EDA
- Very advanced software
  - Example: design rule checking
  - Example: Pentium fdiv bug
- You will learn a lot
- That you can apply at numerous other occasions
  - Abstraction, modeling are key
- Why electrical engineers for EDA?
- You will have to understand the underlying issues!!!
EDA Education Goals

- Show current and future CAD tool users what is going on inside tools
  - Appreciate possibilities and limitations
  - Complexity of problems
- First introduction to students that want to specialize in CAD
- Example of solving complex technical automation problems
  - Useful for other branches of technology
  - Motivation for other algorithm courses
  - Also for Non-EE students

Typical EDA Optimization Setting

Chip optimization problem → ‘Standard’ problem → Standard Algorithm → Problem (approximately) solved → Sub-optimal chip

Transform problem into similar, known, solvable problem in ‘mathematics world’ → ‘bend back’ into real world

Optimization often part of synthesis
Example 1: Steiner Tree

Steiner tree is ‘standard’ abstraction of typical routing applications

Problem: Steiner tree problem is NP complete (as is routing to begin with …)

\[ G = \{a, b, c, d, e\} \]
\[ R = \{a, b, d\} \]

**Determine a Minimum Steiner Tree on R in G**

Solution: cost = 9
Steiner Tree Heuristic (simple)

Input: graph $G = (V, E)$
net $R = \subseteq V$
Output: approximation of MStT on $R$, in $G$
Algorithm:
1. Determine complete distance graph $G_1$ among vertices of $R$. Weight of edge $(v, w)$ is shortest path between $v$ and $w$ in $G$.
2. Determine MST $G_2$ of $G_1$
3. Replace each edge in $G_2$ by corresponding path in $G$. This is $G_3$
4. Determine MST $G_4$ of $G_3$
5. Remove all leaves of $G_4$ which are not in $R$. This is the approximation of MStT.
### Steiner Tree Heuristic (simple)

3. Replace each edge in $G_2$ by corresponding path in $G$. This is $G_3$.
5. Remove all leaves of $G_4$ which are not in $R$. This is the approximation of MStT, $G_5$.

**Cost = 10: Sub-optimal!**

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### Example 2: Handling Trade-Offs

- **Pareto points**
- **Other points**
  - trade-off curve

**Figure 2.3:** Different modules will have different area-delay points. Only the Pareto points are of interest and span up an area-delay trade-off curve for the module. Combining two modules, several areas are possible at equal delays.

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[Dirk Jan Jongeneel]
That’s All

- VLSI Design is challenging
- Issues arise in digital, analog, mixed signal and RF design
- Always want to be at the edge of technologically possible

- Need continuous research and education
ET4255 Programming Contest

This year’s contest will feature Steiner Tree Generation

Given: a (large) set of points

Required: a minimum length connection among a subset of these points

Who can write the fastest program?

\[
G = \{a, b, c, d, e\} \\
R = \{a, b, d\}
\]

Solution: cost = 9 (sub-optimal)
**Node Numbering**

- Essential step during layout-to-circuit extraction
- Layout is composed of rectangles
- Each rectangle has a so-called tile-number.
- Give each rectangle a second number (the net-number) for the electrical net to which it belongs.
- Rules for two-layer simplification:
  - All red is connected (if it abuts)
  - All green is connected (if it abuts)
  - Grey is empty space
- Consider scalability to billions of rectangles.
Algorithm

Input: A corner-stitched layout data structure

Result: Each tile is numbered with node number
 março de 20 de 2005

(n numbers equal if and only if tiles are electrically connected)

\[
\begin{align*}
n &:= 1 \quad \# \text{start with node number } 1 \\
\text{for all tiles } t & \\
\quad \text{if } t \text{ contains interconnect and } t.\text{node} = \text{nill} & \\
\quad \quad \quad \text{then} & \\
\quad \quad \quad \quad \text{extract_node}(t, n) & \\
\quad \quad \quad n &:= n + 1 \\
\text{extract_node}(t, n) & \\
\quad t.\text{node} := n & \\
\text{for all connected neighbors } b \text{ of } t & \\
\quad \text{if } b \text{ contains interconnect and } b.\text{node} = \text{nill} & \\
\quad \quad \quad \text{then} & \\
\quad \quad \quad \quad \text{extract_node}(b, n) & \\
\quad \quad \quad \text{if } b \text{ contains a contact and } b.\text{node} = \text{nill} & \\
\quad \quad \quad \quad \text{then} & \\
\quad \quad \quad \quad \quad o := \text{corresponding tile in other plane} & \\
\quad \quad \quad \quad \quad \text{extract_node}(o, n) &
\end{align*}
\]

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Node Numbering (2)

(find all neighbors of tile in constant time)

Node Numbering (3)

extract node (6,A) 3 4 7 10 13 2
extract node (7,A) 4 8 10 16
extract node (8,A) 4 9 11 17 10 7
extract node (9,A) 4 5 11 8
extract node (17,A) 8 18 23 16
extract node (23,A) 17 24 26 22
extract node (13,A) 6 14 20 12
extract node (20,A) ...

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### Interconnect Parasitics

- Chip Timing dominated by interconnect R, C
- R and C distributed along interconnect
- Need initial, fine-granularity RC mesh
- Huge data sets
- Impossible to analyze directly

#### Need Layout Parasitics Extraction + Model Order Reduction

### Fundamental Approach

Based on Scanline Algorithm

- Operations take place in a narrow band sliding over layout from left to right
- Layout data read in A.L.A.P.
- Circuit data written out A.S.A.P.
- Sublinear memory complexity
- Near-linear time complexity

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Scanline
Interconnect Resistances

- FEM to determine resistances
- Solution only necessary at ‘boundary nodes’
- Model reduction via Gaussian elimination of internal nodes (matrix based)
- FE Mesh ⇔ resistance network
- Gaussian elimination ⇔ star-delta transformation: network based
- Node can be eliminated when all its neighbors are known

### Gaussian Elimination for RC Networks

\[ C_i := C_i + C_x \frac{G_{xi}}{\sum_{n \in X} G_{xn}} \]
\[ G_{ij} := G_{ij} + \frac{G_{xj}G_{xi}}{\sum_{n \in X} G_{xn}} \]

- Gaussian Elimination = Star-delta transformation
- Elmore delay (first moment of impulse response) is preserved
- Also for coupling capacitances
- On-the-fly elimination
SNE Example: Snake RC

Intended circuit

Initial 3D extraction $\Rightarrow$ lumped RC mesh
109 nodes
164 resistors
720 capacitors

SNE circuit results for Snake RC

<table>
<thead>
<tr>
<th>Exact Poles</th>
<th>100 MHz SNE</th>
<th>200 MHz SNE</th>
<th>500 MHz SNE</th>
<th>100 MHz AWE</th>
<th>200 MHz AWE</th>
<th>500 MHz AWE</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.8 $10^{08}$</td>
<td>7.6 $10^{08}$</td>
<td>8.4 $10^{08}$</td>
<td>8.7 $10^{08}$</td>
<td>8.8 $10^{08}$</td>
<td>1.0 $10^{10}$</td>
<td>2.1 $10^{10}$</td>
</tr>
<tr>
<td>9.9 $10^{09}$</td>
<td>8.4 $10^{09}$</td>
<td>8.9 $10^{09}$</td>
<td>8.9 $10^{09}$</td>
<td>1.0 $10^{10}$</td>
<td>2.1 $10^{10}$</td>
<td></td>
</tr>
<tr>
<td>2.4 $10^{10}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SNE simulation results for Snake RC

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Magnitude Y(AB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>1e-4</td>
</tr>
<tr>
<td>100 MHz</td>
<td>1e-5</td>
</tr>
<tr>
<td>200 MHz</td>
<td>1e-6</td>
</tr>
<tr>
<td>1 GHz</td>
<td>1e-7</td>
</tr>
</tbody>
</table>

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Conclusion

- Physical verification of Integrated Circuits
- From geometry (chip layout) to reduced order model (netlist)
- Devices, interconnect (R, C), substrate
- Model Order Reduction as soon as possible
- Consistency of models remains a challenge
- Being used in practice

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## Backup

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>LSI</td>
<td>Large scale integration</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very large scale integration</td>
</tr>
<tr>
<td>ULSI</td>
<td>Ultra large scale integration</td>
</tr>
<tr>
<td>DSM</td>
<td>Deep sub micron</td>
</tr>
<tr>
<td>VDSM</td>
<td>Very deep sub micron</td>
</tr>
</tbody>
</table>
Design Flow Changes

- Identification moves to earlier higher levels, followed in lower levels by equivalence checking and assertion-driven optimizations.
- Design optimized using many constraints with happens-in-time checking and assertion-driven optimization.
- Integration through hierarchical open architecture with industry standard interface for data control.
- Shared data in memory to achieve data access in real-time access to common data across many applications.
- Incremental analysis and optimization.

Required Advance in Design System Architecture

Today 180 nm

Tomorrow 30 nm
IC Industry Economics

Fab costs >> $1,000,000,000

- Time to market is EVERYTHING (nearly)
  - New game station after the Christmas season can mean bankruptcy
- Design has to be right first time
  - Not a second chance
  - Very reliable design procedures needed

Modeling

**model** *(representation)*

/ˈmɒdl/ noun [C]
a representation of something, either as a physical object which is usually smaller than the real object, or as a simple description of the object which might be used in calculations.
- a plastic model of an aircraft
- By looking at this model you can get a better idea of how the bridge will look.
- No model of the economy can predict when the next recession will be.
- Computer models have been used to predict long-term climatic changes.

/ˈmɒdl/ verb [T]
to model animals out of clay
to model clay into animal shapes
- The whole car can be modelled on a computer before a single component is made. [T]

( *Cambridge International Dictionary of English*)
Modeling

- An abstraction of (the properties) of something to help understanding and predicting its behavior
- Domain Specific: weather, climate, economy, stock market, ...
- Different models for something to answer different questions
- Black-Box modeling vs. Physically Based

- After Einstein: [a model] should be as simple as possible, but not simpler

Abstraction/Modeling is key enabling factor in the success (E)E.